A flexible FPGA based QDC and TDC for the HADES and the CBM calorimeters

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TWEPP 2016, Karlsruhe

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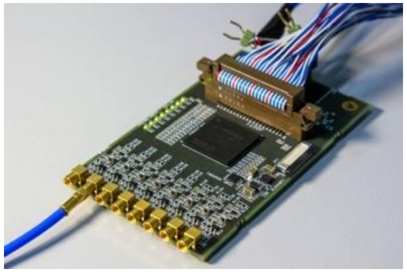
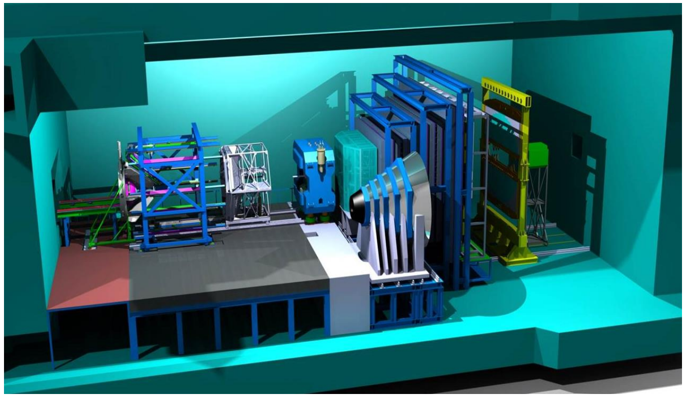
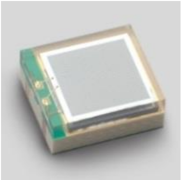
= 

PaDiWa-AMPS
front-end



PMT



Si-PM (MPPC)

Adrian Rost
for the **HADES** and **CBM**
collaborations

GSI HADES CBM

Outline

- **Motivation for a PMT read-out application**
  HADES electromagnetic calorimeter (ECAL) upgrade

- **The QDC and TDC measurement principle**
  PaDiWa-AMPS front-end for the TRB3 platform

- **PaDiWa-AMPS performance for PMT read-out**
  Laboratory measurements
  ECAL module tests with secondary gamma beam at the MAMI facility

- **Adaption for Si-PM read-out**
  CBM Projectile Spectator Detector (PSD) ≈ NA61/SHINE PSD at CERN

- **Summary and outlook**

HADES (High-Acceptance Dielectron Spectrometer) at GSI, Darmstadt, Germany

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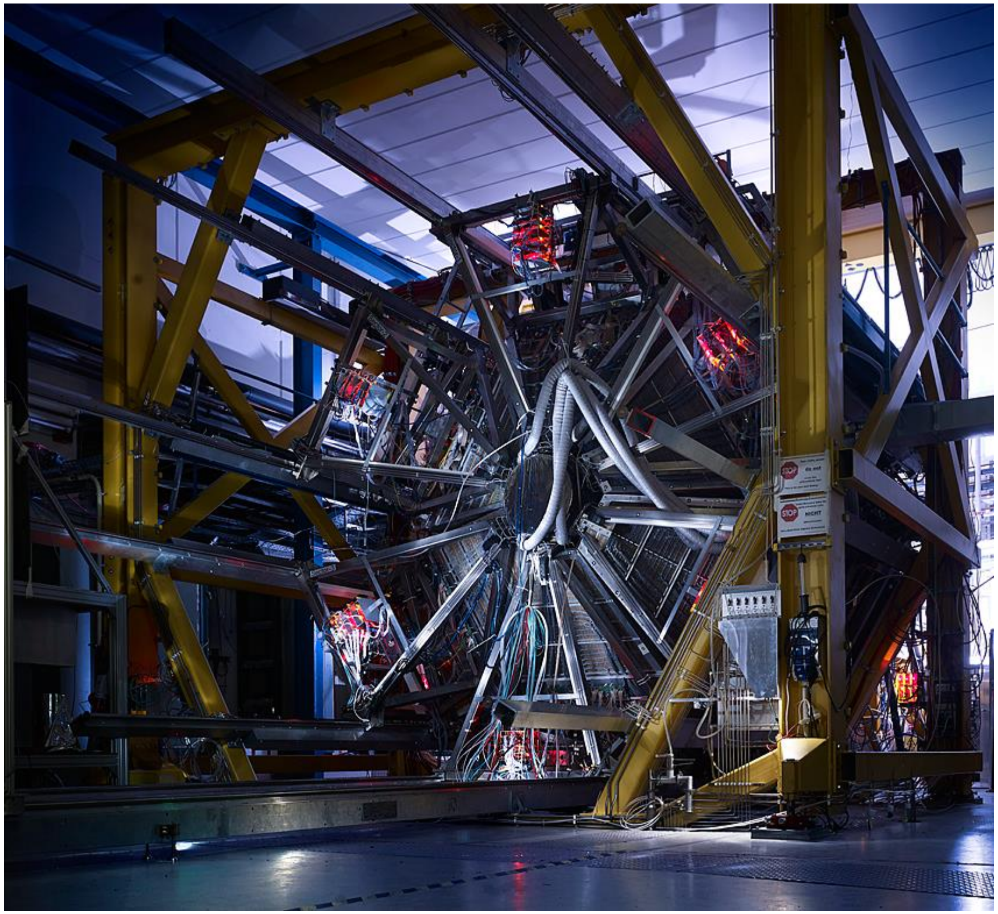

HADES strategy:

- Excitation function for low-mass lepton pairs and (multi-)strange baryons and mesons
- Various aspects of baryon-resonance physics

HADES (High-Acceptance Dielectron Spectrometer) at GSI, Darmstadt, Germany

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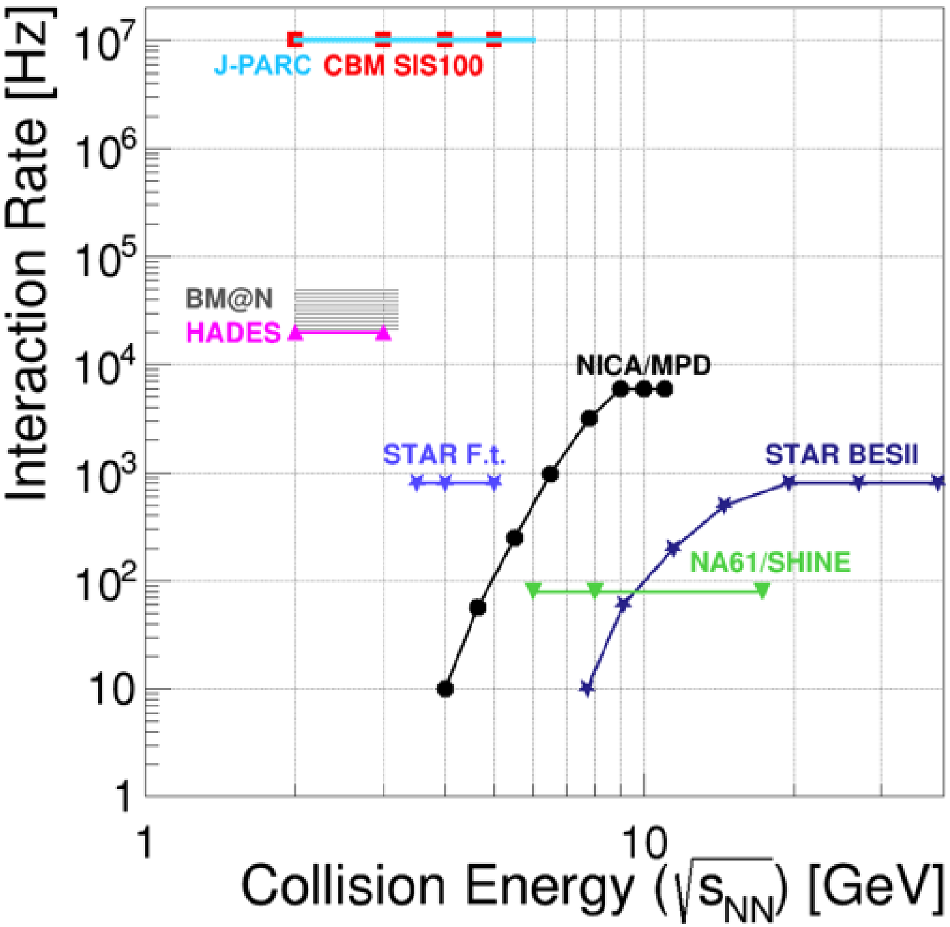


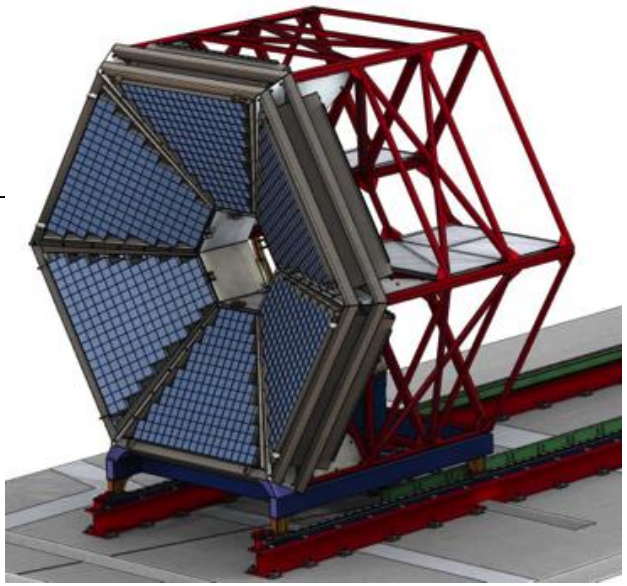
HADES strategy:

- Excitation function for low-mass lepton pairs and (multi-)strange baryons and mesons
- Various aspects of baryon-resonance physics

- Fixed-target, high interaction rate experiment

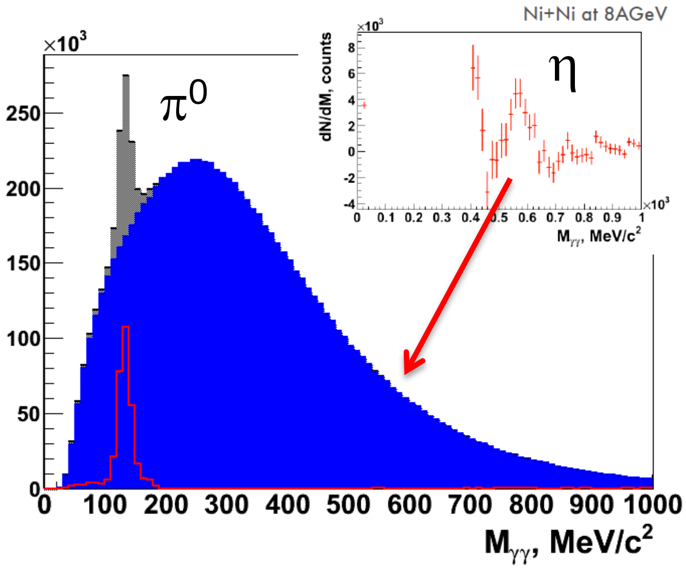
- 2002–2009: light A+A, p+p, n+p, p+A
- 2011–2014: Au+Au, π-induced reactions
- 2018–2020: FAIR phase 0 → high-statistics π+p/πA, p+A and A+A

Motivation for an ECAL upgrade in the HADES experiment at GSI (Darmstadt)



Planned for SIS18 at GSI and SIS100 at FAIR

- 978 modules of lead glass + photomultiplier
- Polar angle coverage: 12° - 45°
- **Novel read-out electronics concept**



- Measurements of π^0 and η via $\gamma\gamma$-decay channel
  → E_{kin} = 2 – 11A GeV no measurements exist
- Spectroscopy of $\Lambda(1405)$ and $\Sigma(1385)$
- Measurement of a_1 spectral function
- Better electron/pion suppression for large momenta (p>400 MeV/c)

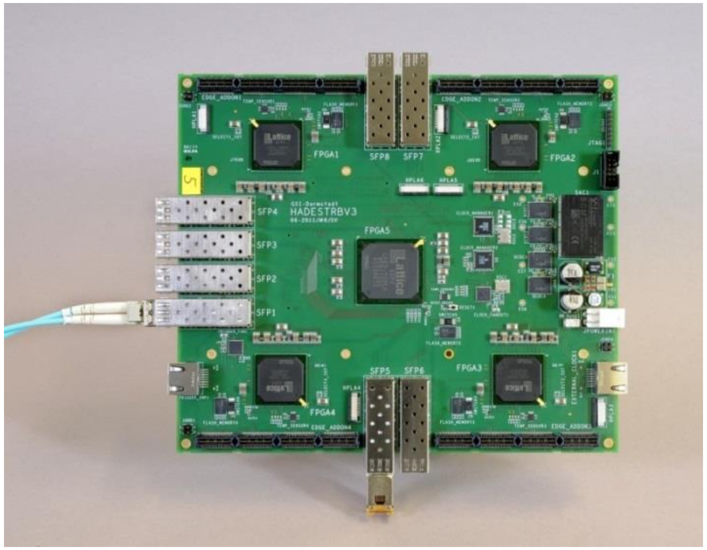
TRB3 platform

FPGA TDC and multi purpose DAQ

Time precision
8 ps RMS

C. Ugur et al. “A novel approach for pulse width measurements with a high precision (8 ps RMS) TDC in an FPGA”, *JINST*, vol. 11, no. 01, p. C01046, 2016.

4 FPGAs with
260 TDC channels



Single edge & ToT measurements

Usable in large systems & stand alone

50 MHz hit rate per channel

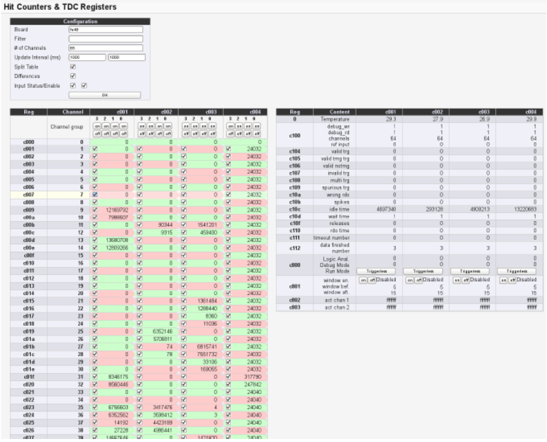
Only **48 V** and GbE needed to take data

Internal trigger system and slow control

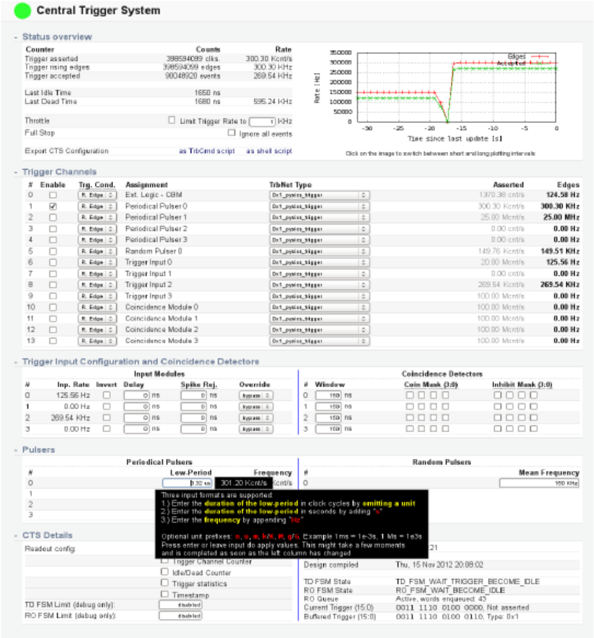
Expandable by several Add-Ons and FEEs
→ i.e. PaDiWa-AMPS

(developed at GSI, see: http://trb.gsi.de/)

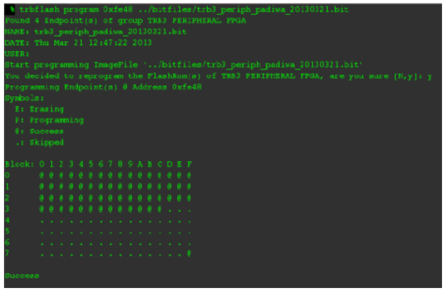
TRB3 Software Package



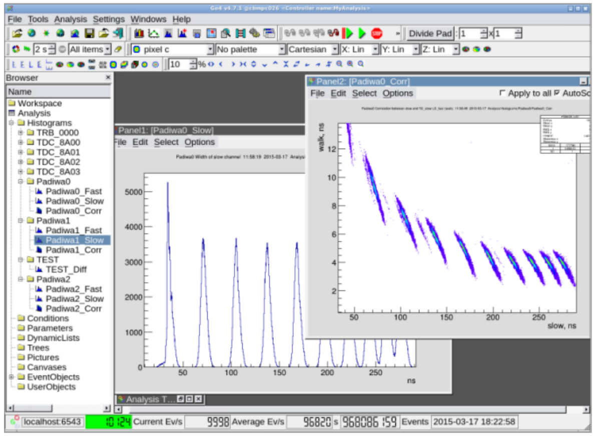
TDC channels monitoring & control



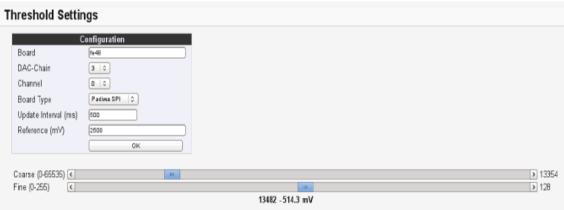
Central trigger system



Console based slow control



Unpacking & online analysis tools *(see: go4.gsi.de)*

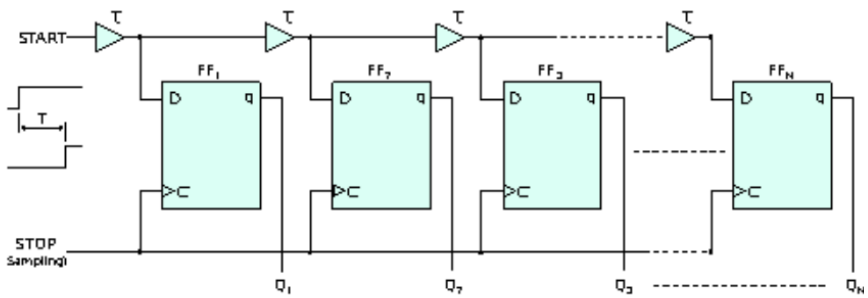


Threshold settings

FPGA used as TDC and discriminator

FPGA TDC:

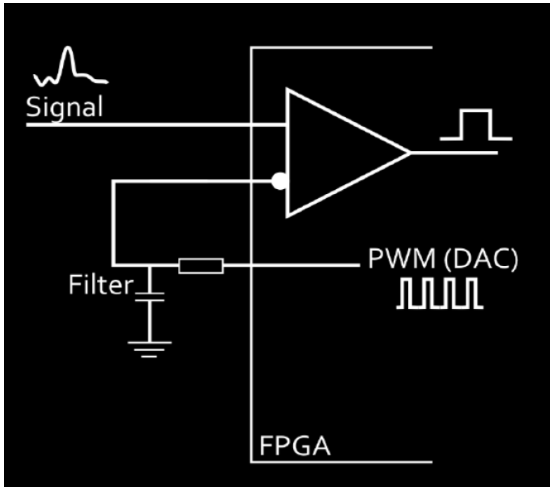
- TDC method: tapped delay line with common stop (200 MHz clock)
- Delay elements realized by LUTs
- Sampling is realized by registers



J. Kalisz, Review of methods for time interval measurements with picosecond resolution, Metrologia, 2004.

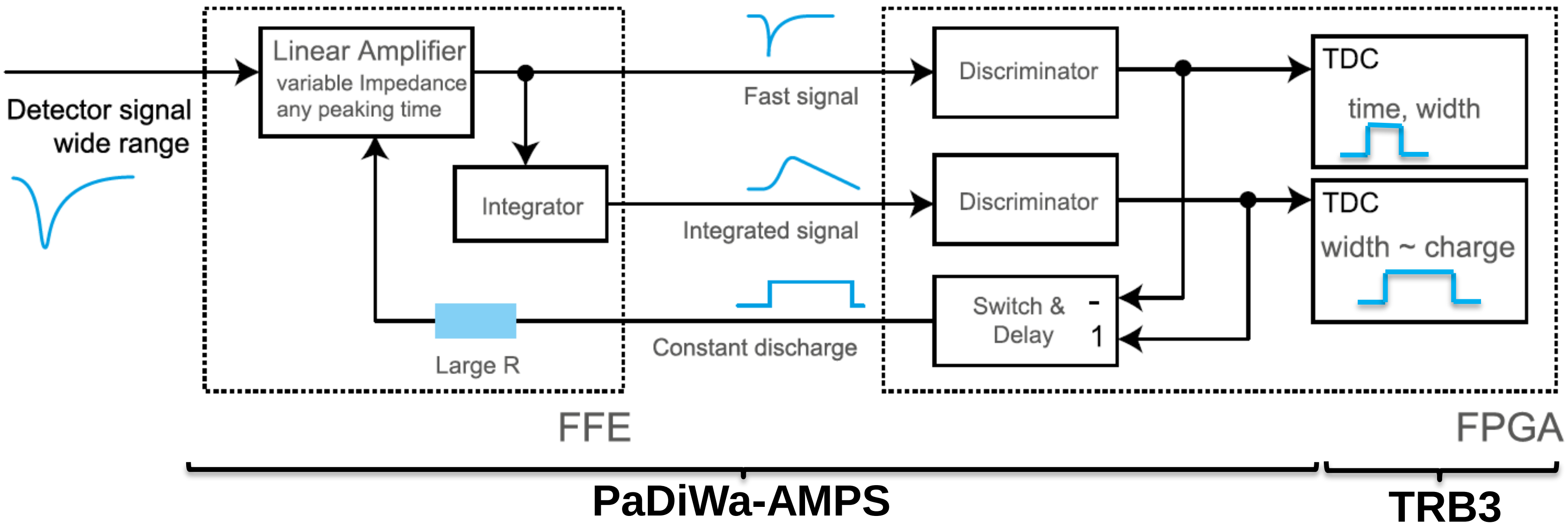
FPGA discriminator:

- LVDS input buffers used as comparator
- Leading edge and ToT is encoded in a digital signal
- Thresholds are set via PWM and a low pass filter



The COME & KISS* charge and time measurement principle: *Modified Wilkinson ADC*

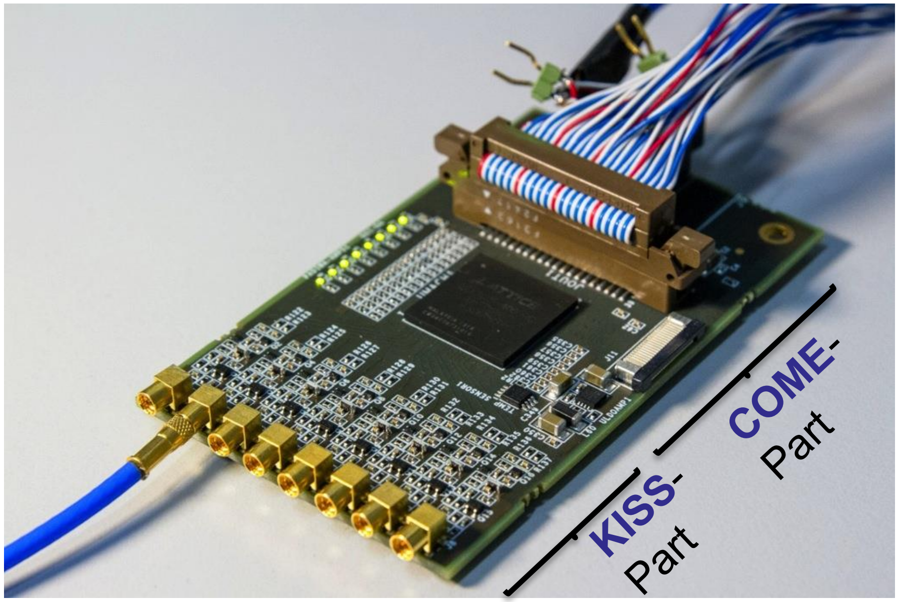
* use **com**mercial **e**lements and **k**eep **i**t **s**mall & **s**imple

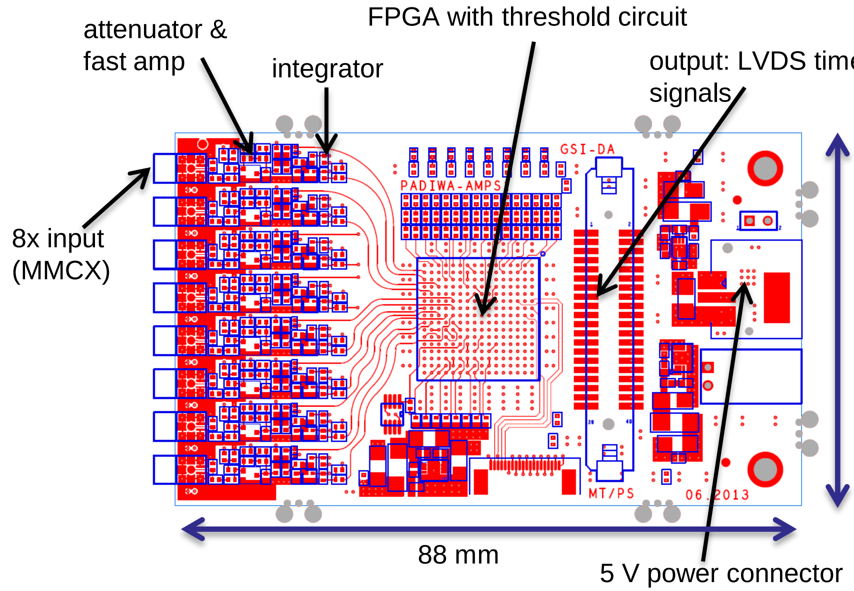


- Input signal is integrated with a capacitor
- Capacitor is discharged using a constant current source triggered by the input signal

→ Measure ToT of integrated signal ~ **charge**
→ Measure leading edge of fast signal ~ **timing**

PaDiWa-AMPS front-end prototype board for the TRB3 platform



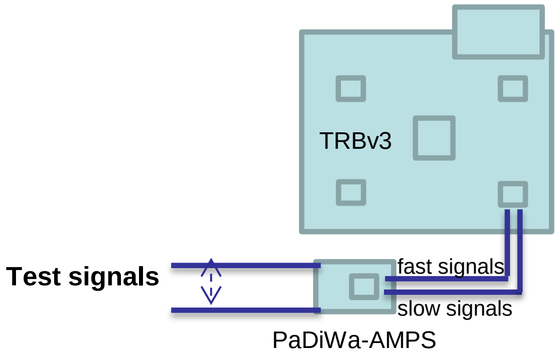


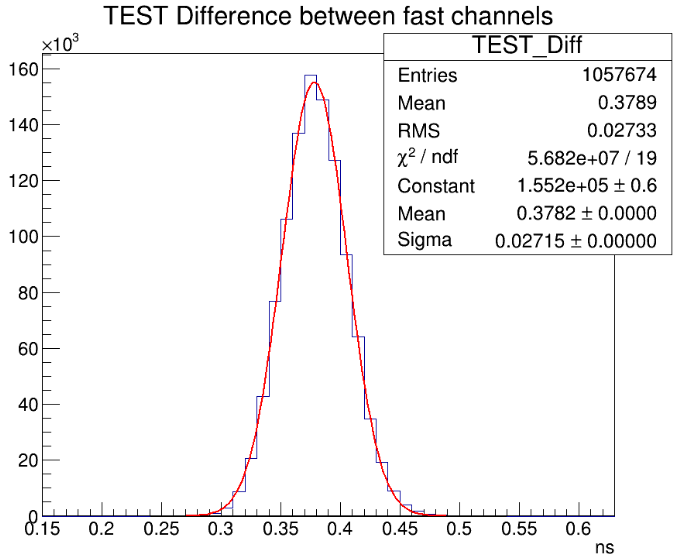
- **1** Lattice Lattice MachXO2-4000 FPGA
- **8** MMCX input channels → at least 16 TDC channels on TRB3 (using the multi-hit TDC functionally)
- Time Precision: **~ 19 ps**
- Relative charge resolution: **< 0.5 %** (for pulser signals >1 V)
- Dynamic range: **~ 250**
- Max. rate capability: **~ 100 kHz** (optimization ongoing!!!)
- Power consumption: ~**1.5 W**
- *Universal read-out applications due to the flexible analog part*

Time precision for pulser measurements

- PMT like pulser signal as input into PaDiWa-AMPS
- Measured was the jitter between fast_LE of two PaDiWa channels

→ Time precision (characterized by sigma) of about **~ 27 ps / $\sqrt{2}$ = 19 ps**

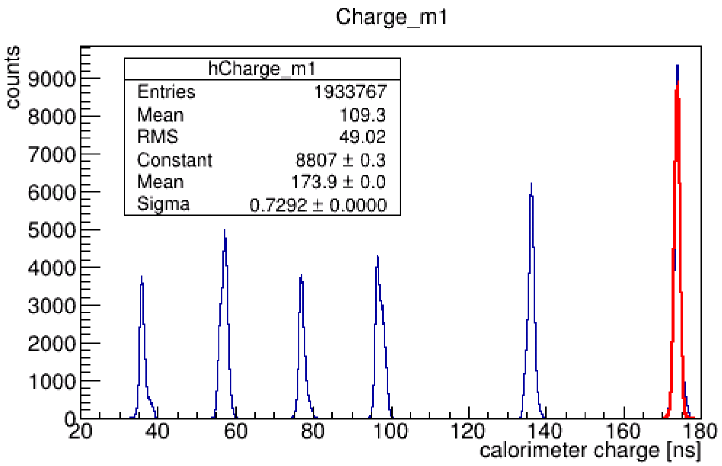


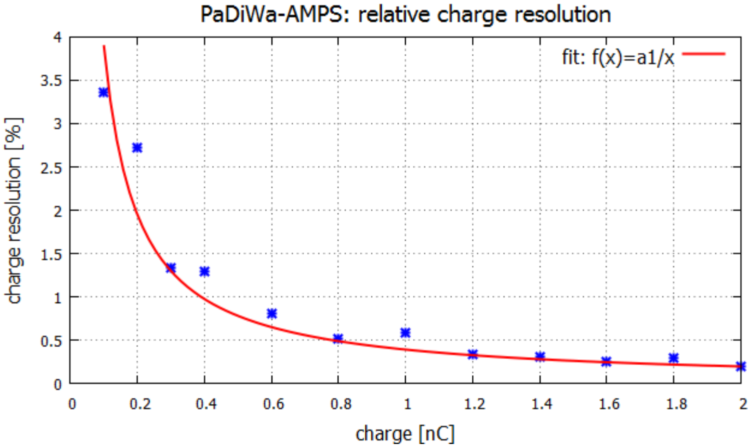


Charge resolution for pulser measurements (without walk correction)

- Charge-to-width (Q2W) measurement for different signal widths (~ charges) generated by pulser
- Relative charge resolution depends on attenuation resistor, for expected ECAL signals is below **0.5%**

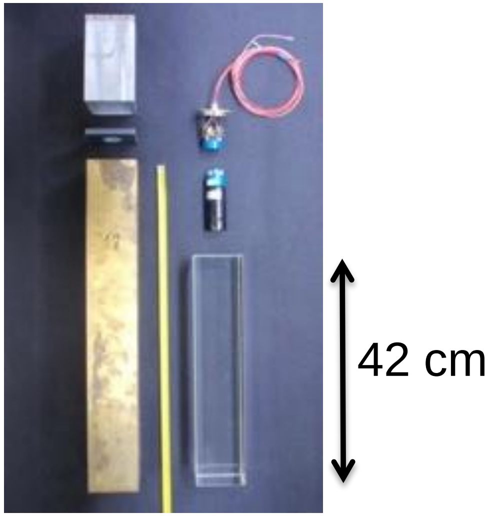
→ Walk correction can still improve the relative resolution



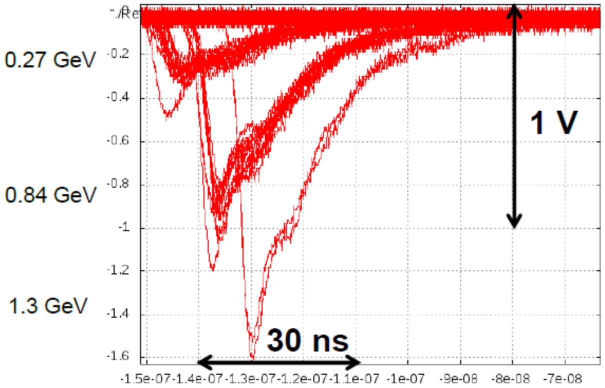


PaDiWa-AMPS under beam conditions:
Calorimeter PMT read-out

HADES ECAL module
- EM shower produces Cherenkov light in the lead glass
- Read out by 1.5″ EMI 9903KB and 3″ Hamamatsu R6091 PMTs



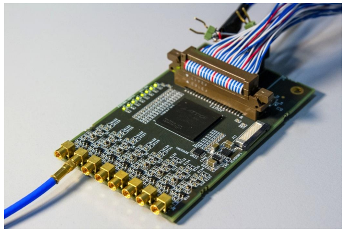
Beam-time at MAMI facility in Mainz
- Secondary gamma beam: E_{γ} ~ (100 – 1400) MeV
- Test of ECAL modules with 1″, 1.5″ and 3″ PMTs

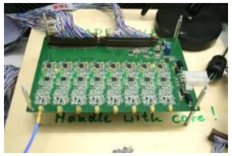


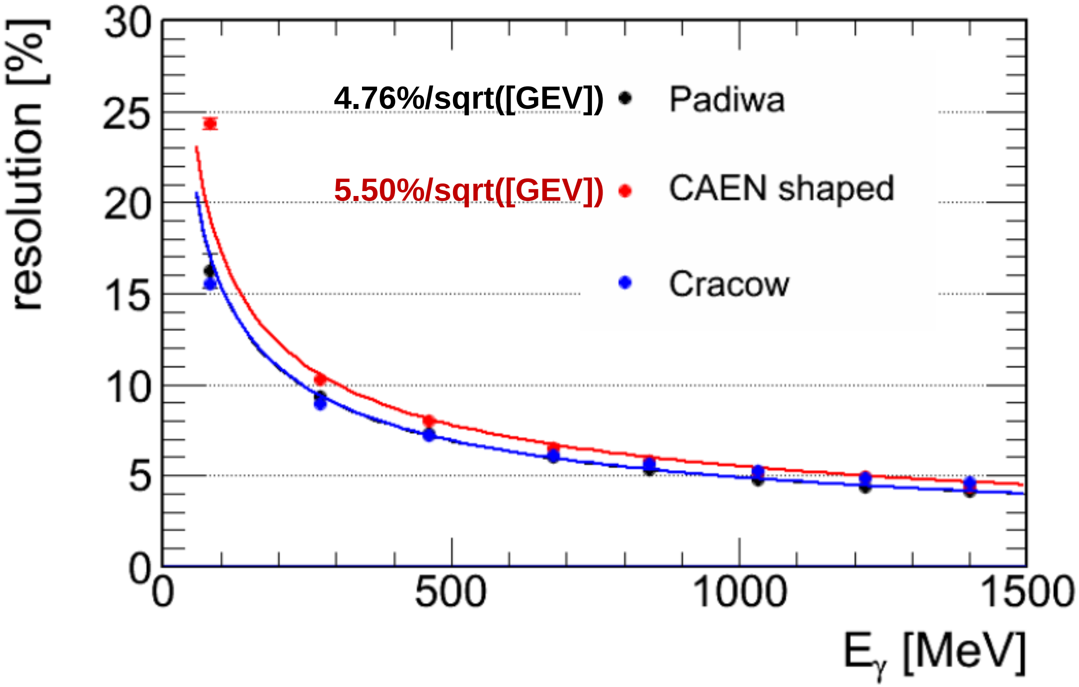
Signal key facts:
- Signal amplitude: 50 - 2000 mV
- Signal rise time: ~2 ns, width: ~ 50 ns
- Rate: ~ 5 kHz (100 Hz trigger)

Relative energy resolution of an ECAL module

3″ Hamamatsu PMT



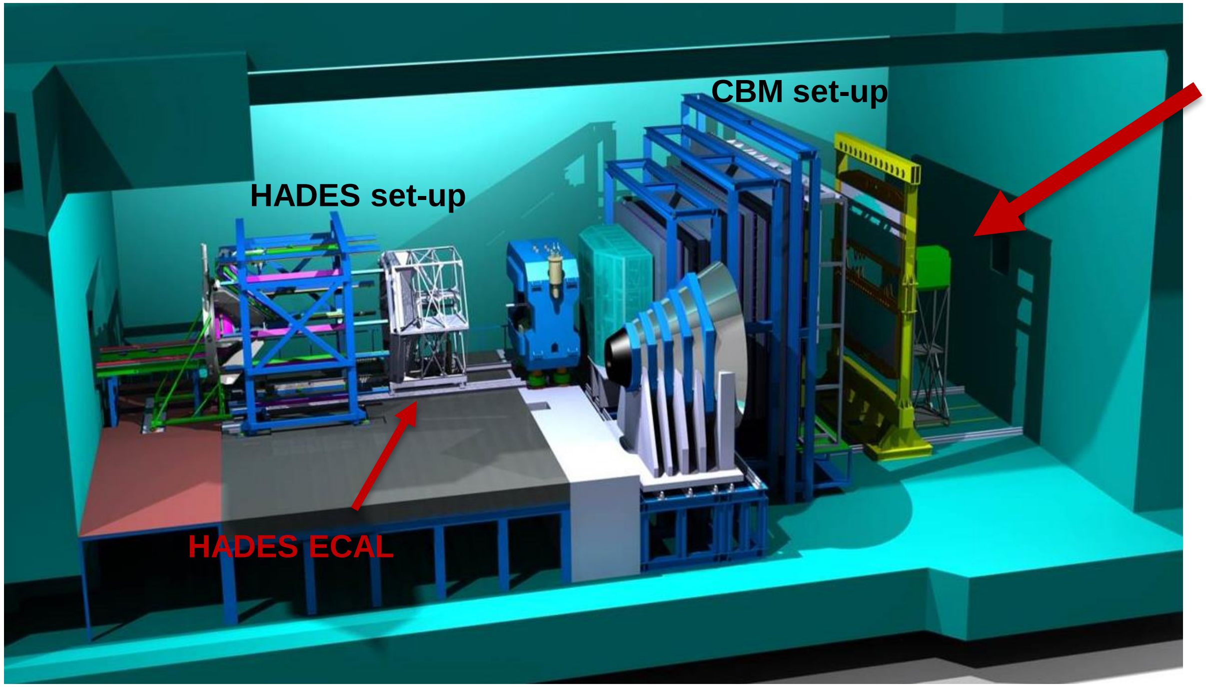




- PaDiWa-AMPS Q2ToT
- "Cracow" ADC
- Reference: CAEN DT5742
  5 GS/s Waveform digitizer with
  GSI MA8000 shaper

→ **Measurements are in line with reference CAEN system**

The Projectile Spectator Detector (PSD) of the CBM experiment at FAIR



Future location: FAIR, Darmstadt, Germany

Projectile Spectator Detector (PSD)

Determination of:

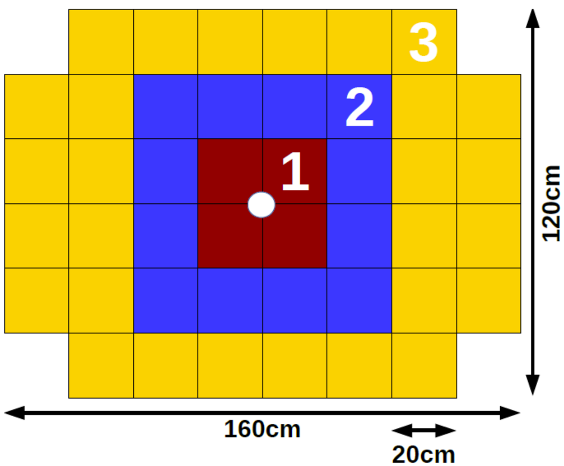
- Collision Centrality
- Event-plane

→ Measure energy distribution of projectile nuclei fragments (spectators) by a hadron calorimeter

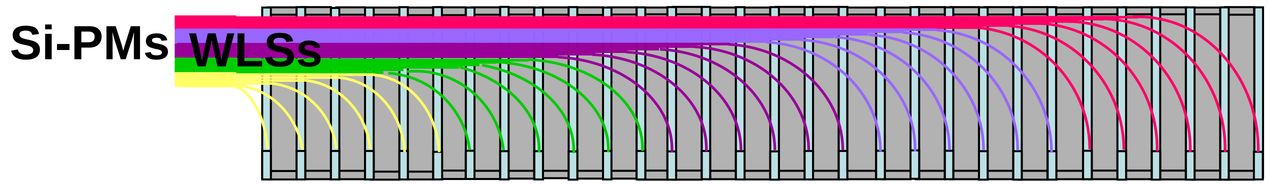
CBM PSD structure

Lead-scintillator sandwich hadron calorimeter

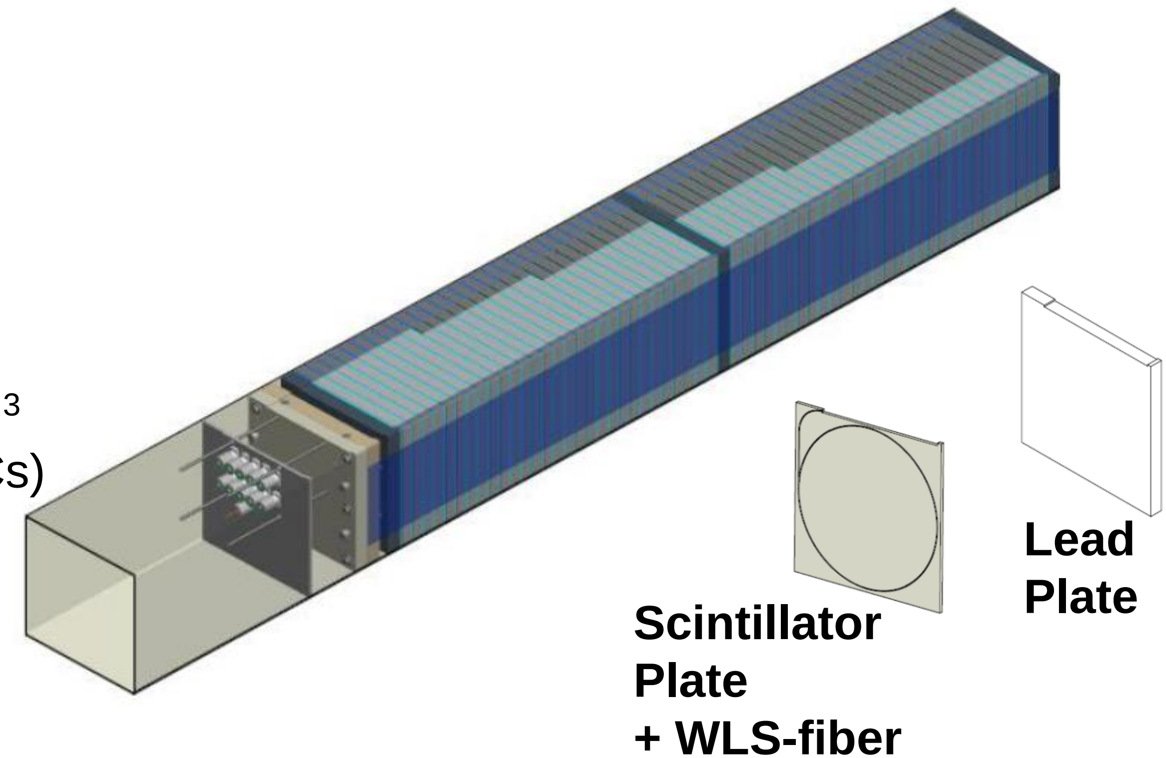
PSD front view

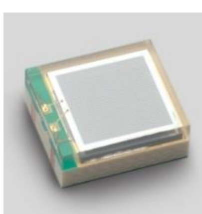


Top view of ½ module



- 44 modules a 60 sections
- Dimensions: 20x20x120 cm^3
- Readout via Si-PMs (MPPCs)

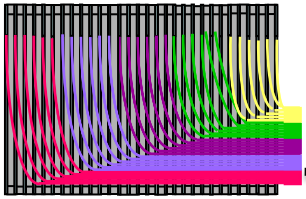




Si-PM
Hamamatsu S12572-010P MPPC

PaDiWa-AMPS test read-out scheme of the NA61/SHINE PSD

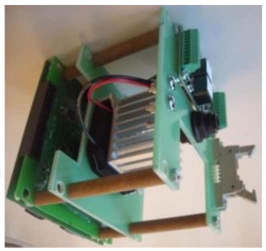
PSD module



- 1 module with 10 sections

WLS fibers

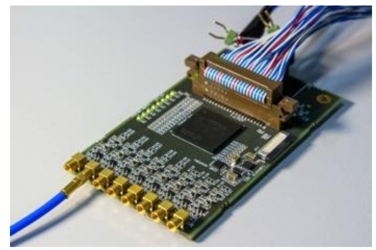
10 Si-PMs + Preamplifier



- Temp. control
- HV control

Coax. (50 ohms)

2 PaDiWa-AMPS front-end boards



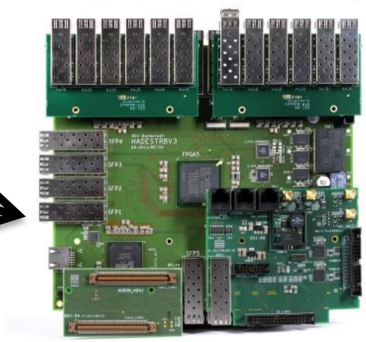
- Q2ToT conversion
- FPGA-discriminator

LVDS

ext. Trigger

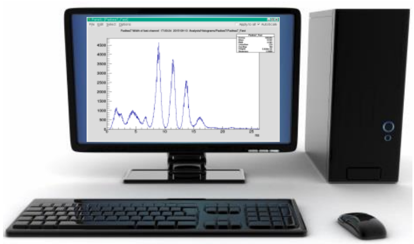
NIM

TRBv3



- FPGA-TDC

Gigabit Ethernet



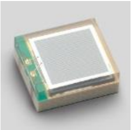
DAQ PC

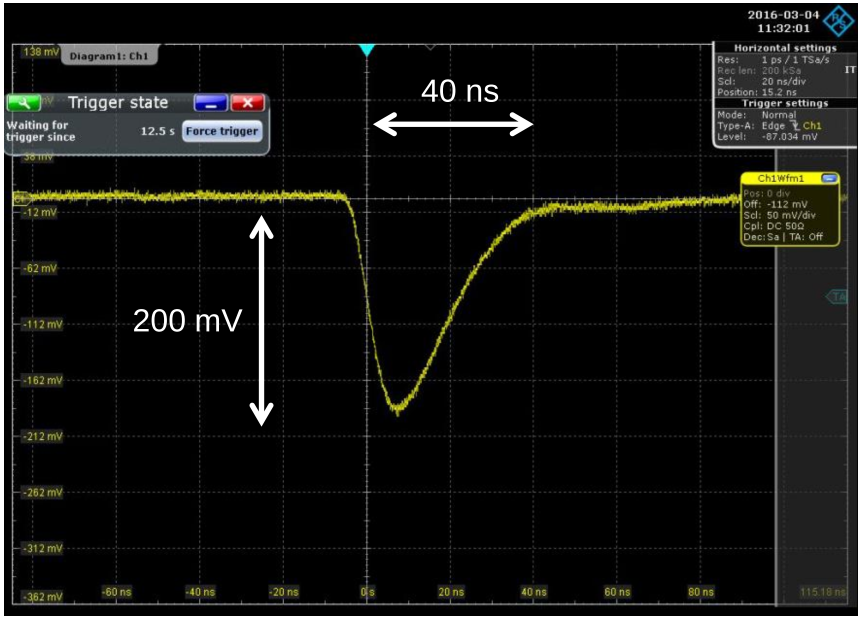
PSD of the NA61/Shine experiment at the CERN SPS

module structure is identical to the CBM PSD

PSD read-out requirements/challenges

Hamamatsu S12572-010P MPPC
 + NA61 pre-amplifier
irradiated with a LED flash





<u>Signal key facts:</u>

- Signal amplitude: 5 mV – 2000 mV
- Signal rise time: ~10 ns, width: ~ 40 ns
- Rate: up to 1 MHz (in CBM PSD)
- noisy signals

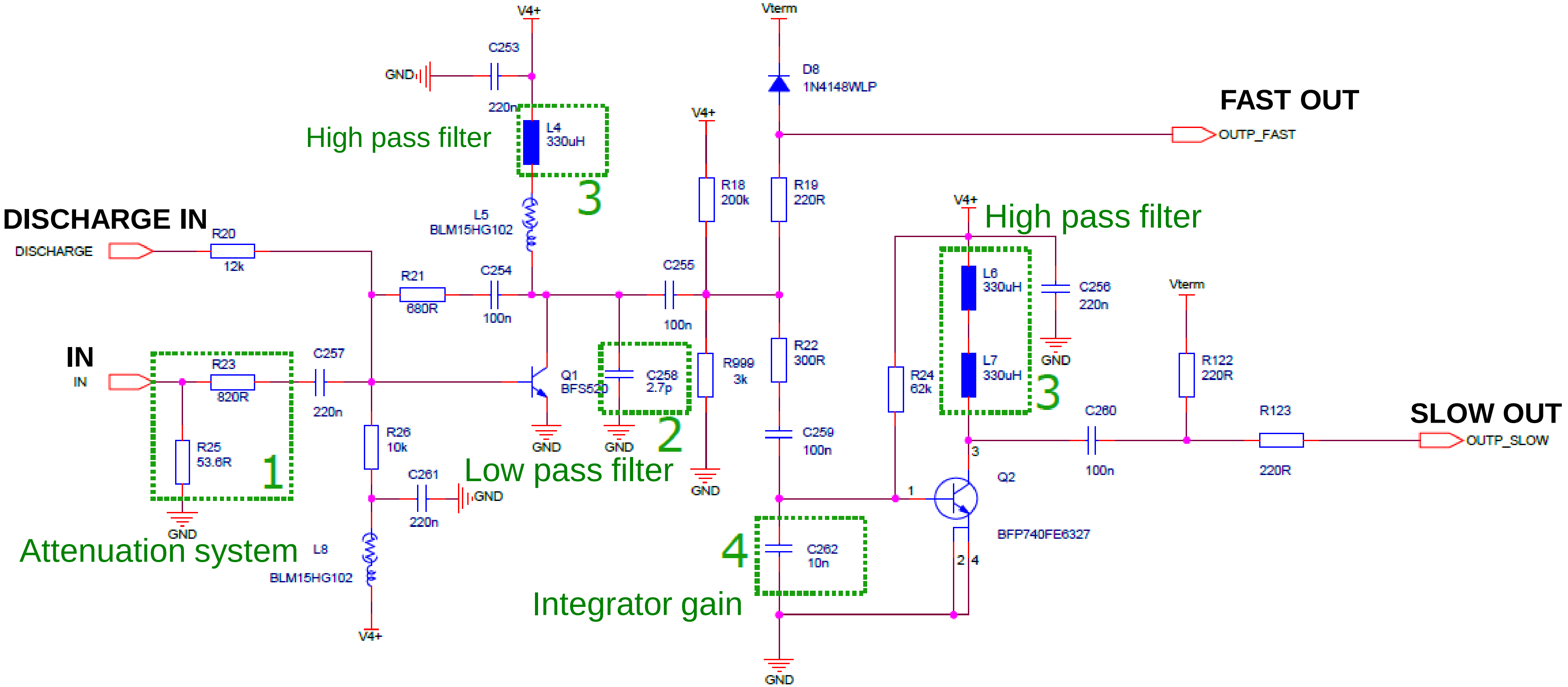
→ Adaption of the PaDiWa-AMPS analog stage needed

→ Challenging dynamic range

→ Proper filtering of noise needed

PaDiWa-AMPS flexible KISS analog schematics

Analog stage without FPGA



- Amplification and S/N ratio can be easily adapted to different detector pulse shapes by changing some resistors, capacitors and inductors

→ Cross checked via SPICE simulations and laboratory measurements

First steps towards SiPM read-out of the NA61/SHINE PSD

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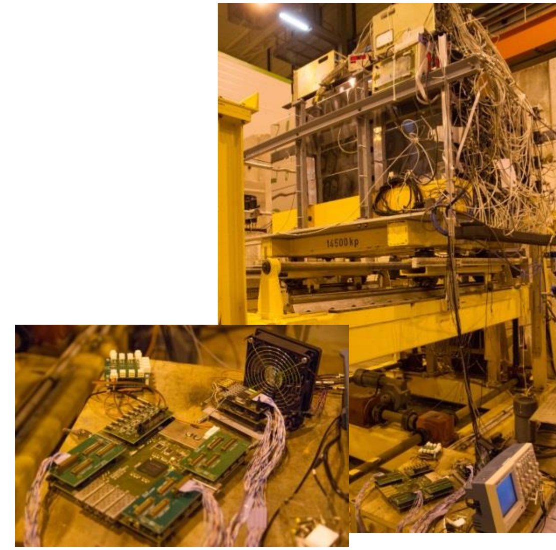
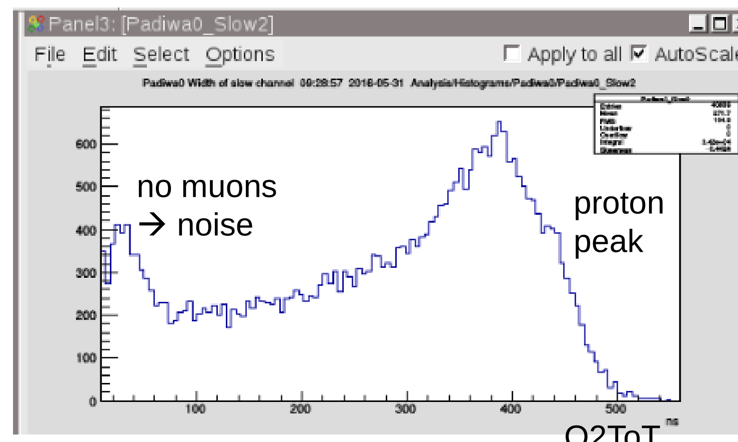
- Modified PaDiWa-AMPS used to read-out one module (10 SiPMs) of the NA61/SHINE PSD
- Proton beam at 60 GeV/c
- Proton peak is clearly visible
- Muon peak which is used for calibration is not visible because of to bad S/N ratio

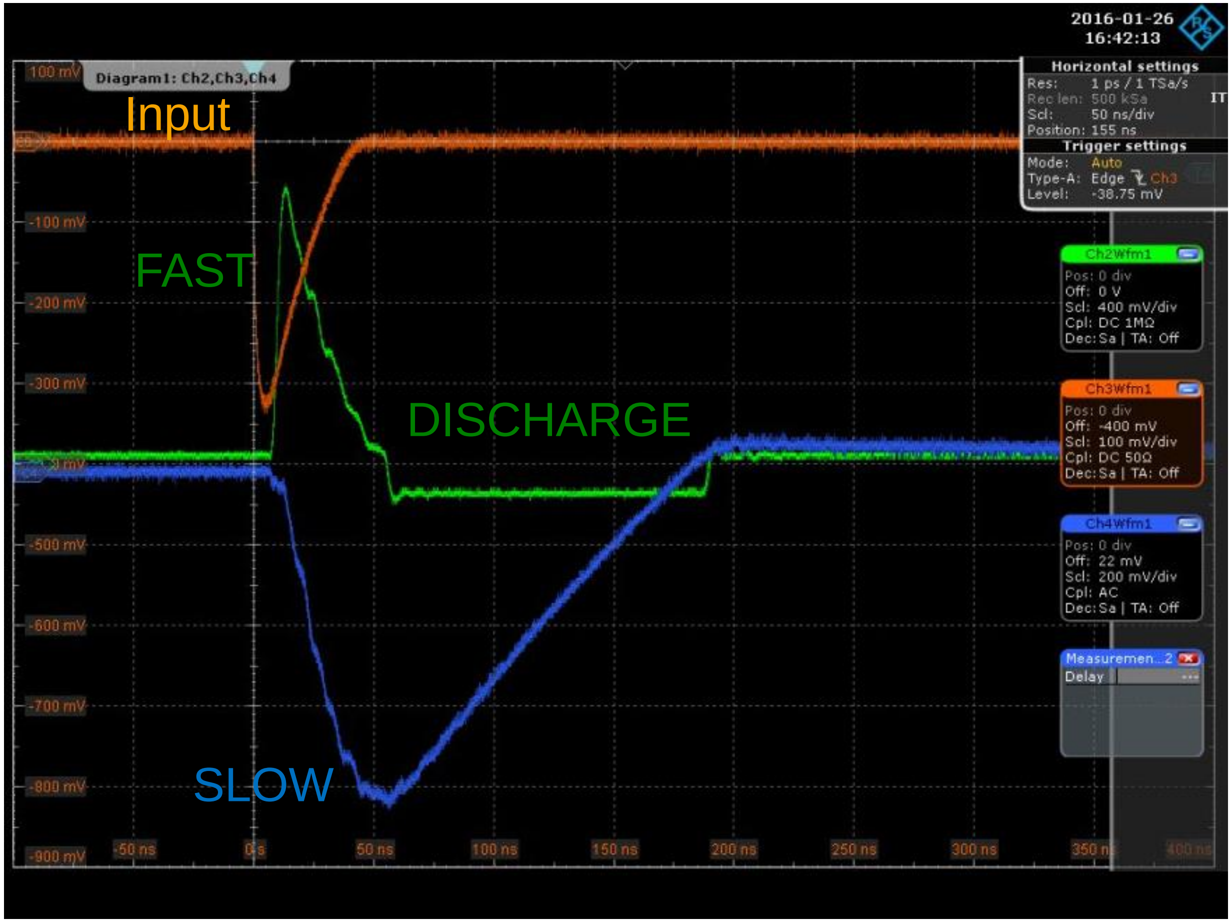
→ Better adjustment of the PaDiWa-AMPS band-pass filters needed
or/and
improvements in pe-amplifier+SiPM





Optimization of the DISCHARGE generation

More flexibility for different pulse shapes (width)



- DISCHARGE is used to discharge the integration capacitor
- Start triggered by a logical **&** between the integrated discriminated SLOW signal and a delayed discriminated FAST signal

→ Should be matched to the input signal width

Start of the DISCHARGE is delayed inside the FPGA via routing

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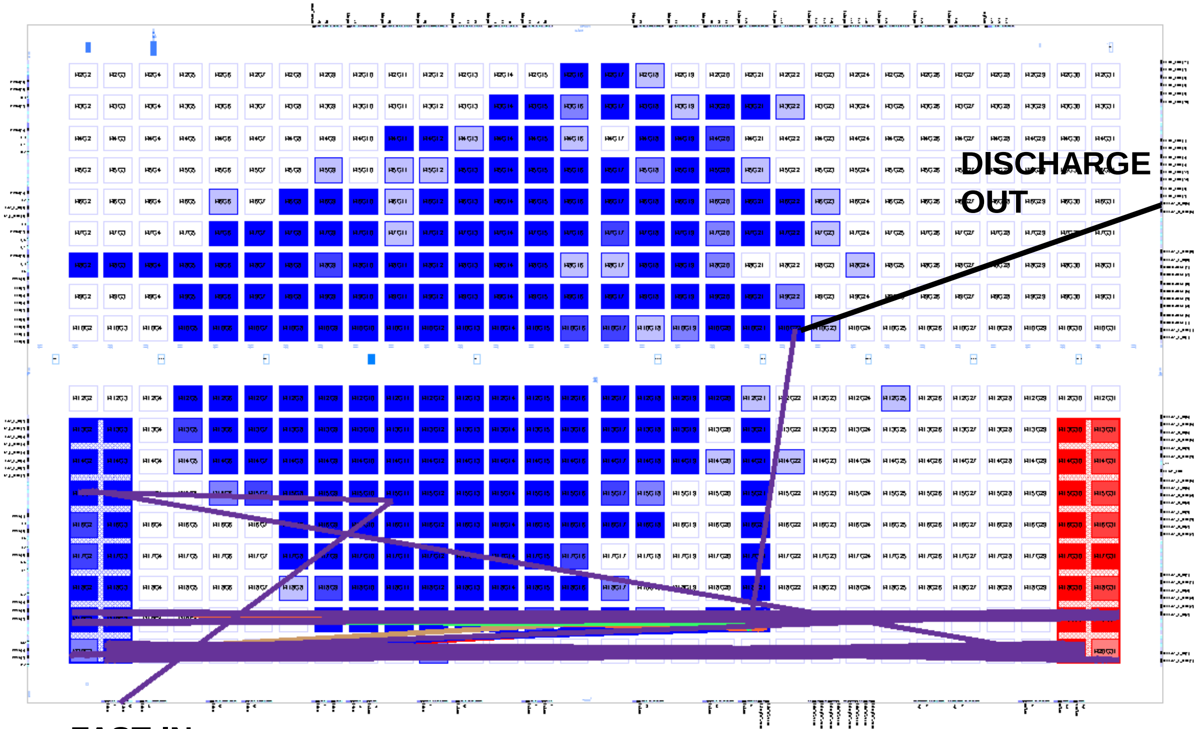
FPGA floorplan view and placement of the instances

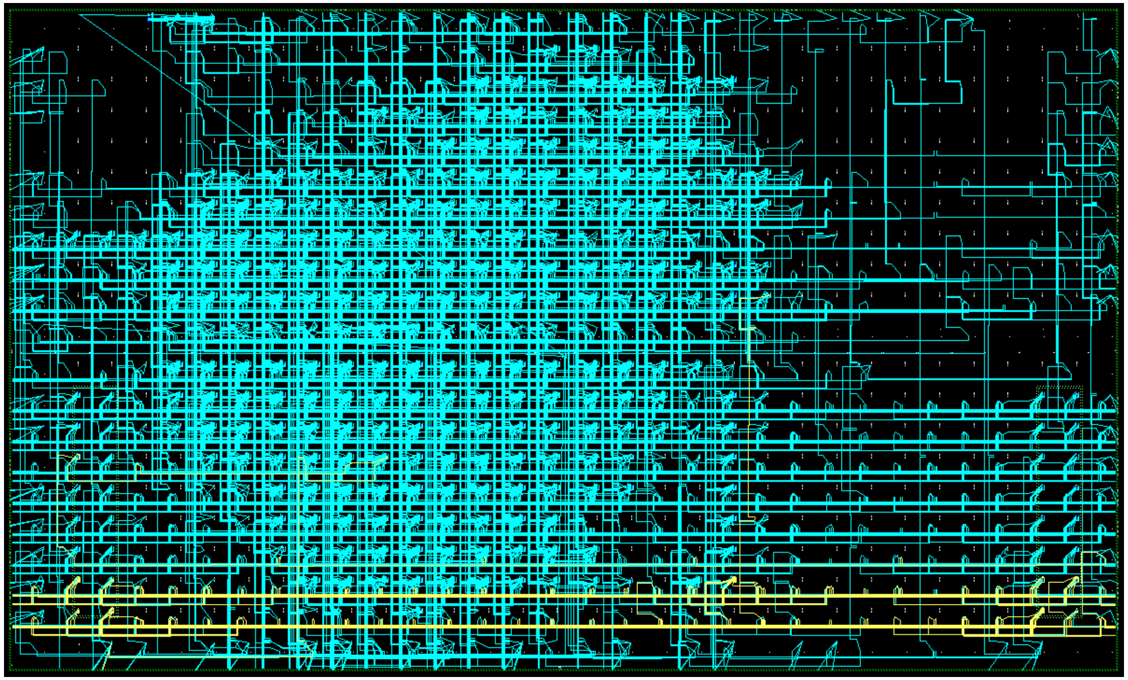


- Multiplexer allows the selection of delay lines which generate an delay of **15 ns - 65 ns**

→ Longer delays can be easily added, shorter delays are possible with optimized placement

Start of the DISCHARGE is delayed inside the FPGA via routing

FPGA physical view showing the connection of the instances



DISCHARGE OUT

FAST IN

- Multiplexer allows the selection of delay lines which generate an delay of **15 ns - 65 ns**

→ Longer delays can be easily added, shorter delays are possible with optimized placement

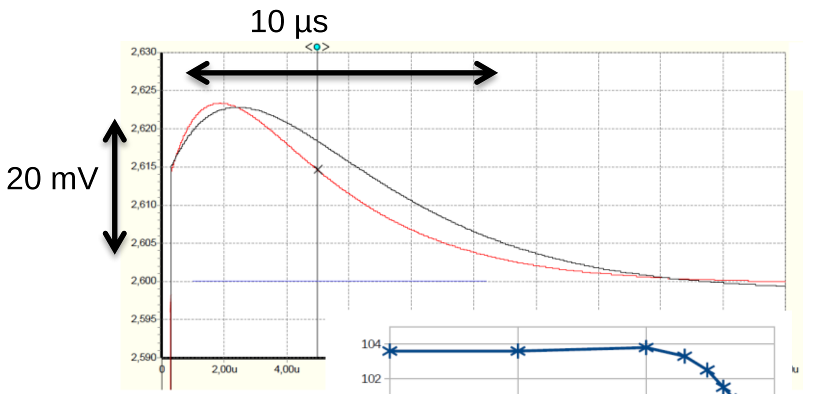
Summary and Outlook

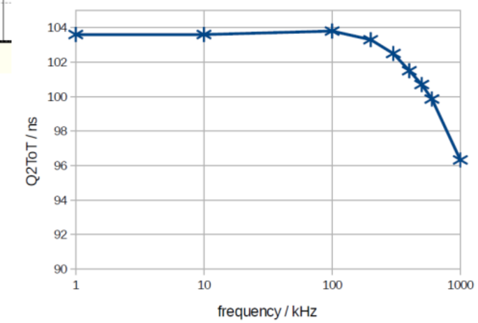
PaDiWa-AMPS TDC and QDC principle is working and proven:

✓ Laboratory
  → Time precision of ~**19 ps**,
  → Electronics resolution **<0.5%** (for ECAL signals > 1 V)
  → Dynamic range: **~250**

✓ ECAL energy resolution tests at MAMI
  → Results are in agreement with reference DAQ

✓ First steps towards an adaption to SiPM signals
  → noise problems have to been solved





Outlook:

- Implementation of an active baseline restorer in the FPGA to increase rate capability
- Further S/N ratio and timing improvements
- Adaption to detector signals with pulse width < 20 ns (MCP, diamond detectors)

→ **Redesign of a new board is currently ongoing**
→ **Further beam tests i.e. at NA61/SHINE**

Thank you for your attention!!!
…and stay tuned!

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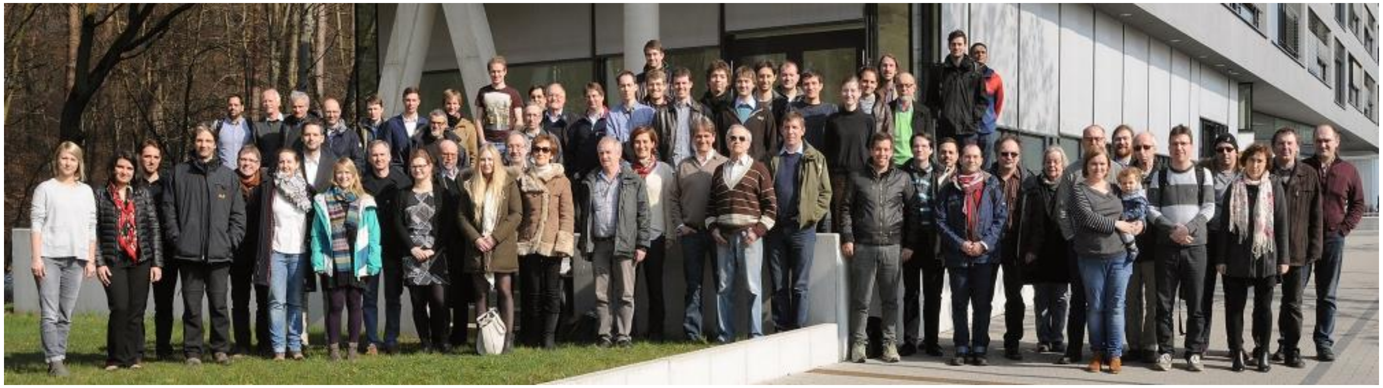

HADES

CBM