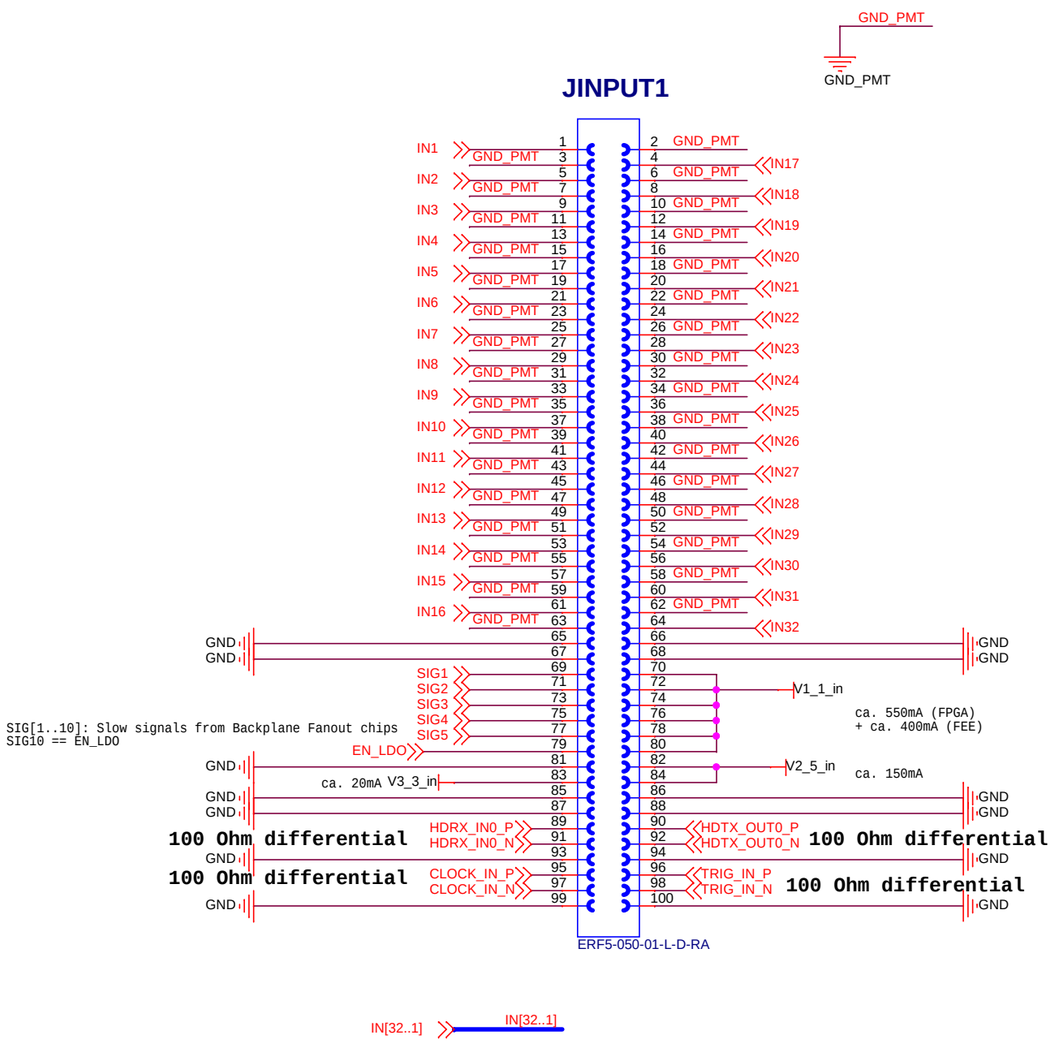
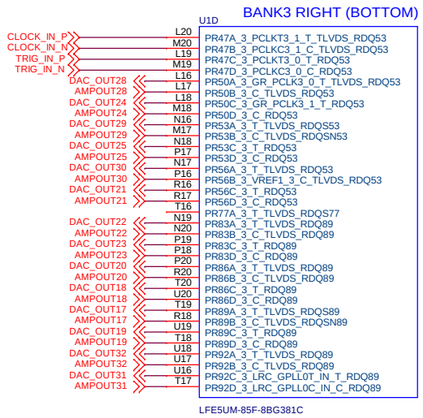


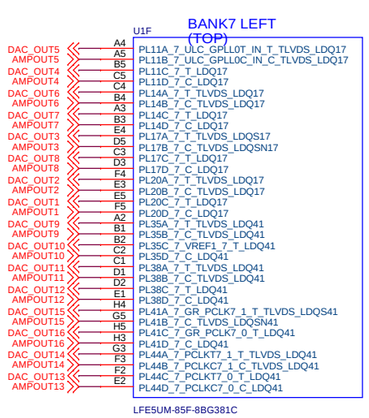
Gesellschaft für Schwerionenforschung mbH
Planckstrasse 1
D-64291 Darmstadt
GERMANY
www.gsi.de

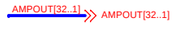
<Title>

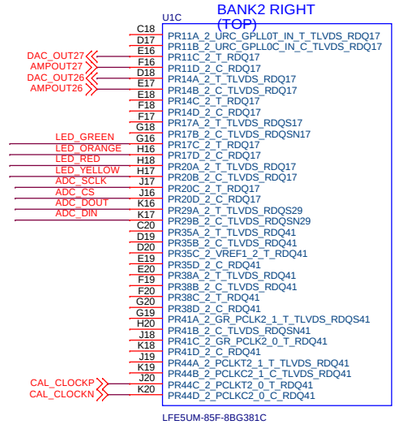
Design: K:\GSIJOB\COME_AND_KISS\DIRICH\DIRICH1\DIRICH1.DSN	
Modified: Tuesday, March 15, 2016	Size: A3 Page: 1 / 8
Designer: <Designer>	Layouter: <Layouter>

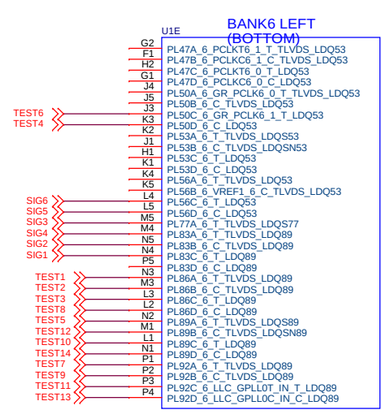
Bank 0,1,4,8: no true LVDS inputs
Bank 2,3,6,7: LVDS inputs, 50% LVDS outputs



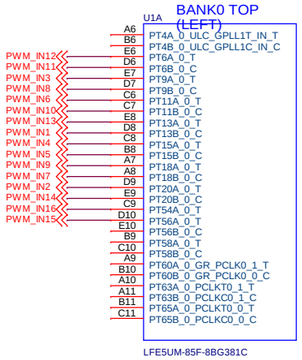


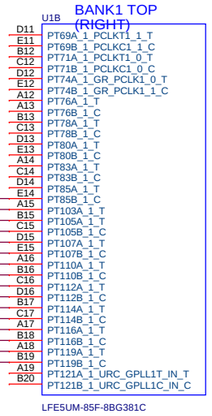


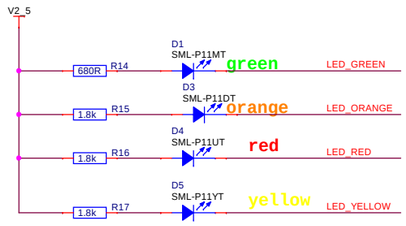




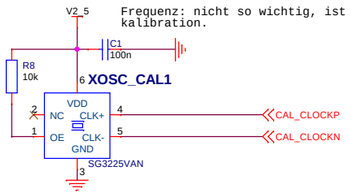
Bank 0,1,4,8: no true LVDS inputs

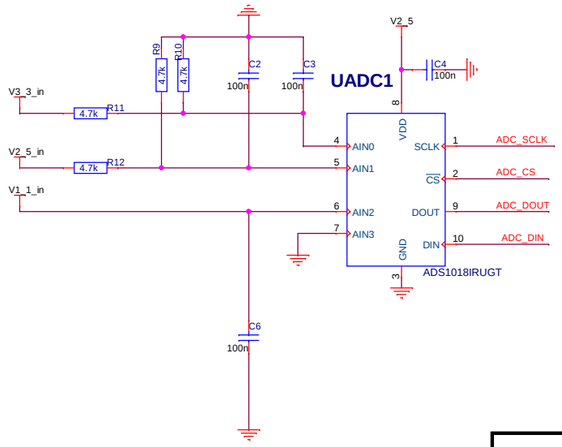


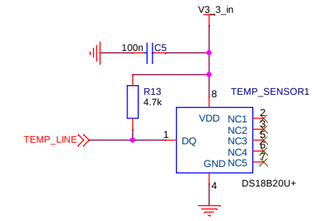




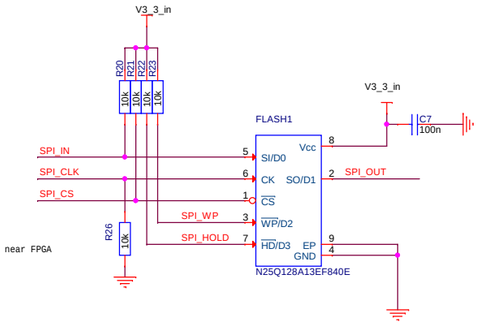
Part No.	Resin Color	Forward voltage V_F		Reverse current I_R		Light wavelength Dominant λ_D		Brightness I_V		
		Typ. (V)	I_F (mA)	Max. (µA)	V_R (V)	Typ. (nm)	I_F (mA)	Min. (mcd)	Typ. (mcd)	I_F (mA)
SML-P11MT	Transparent Colorless	1.9				569		0.63	2.1	
SML-P11YT		1.9				586		2.5	7.6	
SML-P11DT		1.8	1	100	4	605	1	2.5	7.3	1
SML-P11UT		1.8				621		1.6	5.5	
SML-P11VT		1.8				626		1.0	3.6	

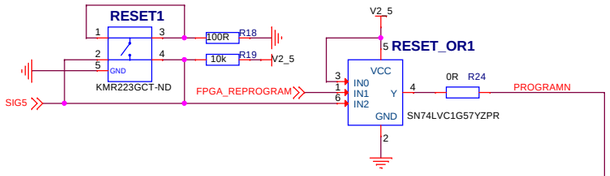




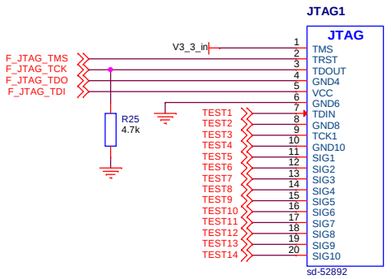


Gesellschaft für Schwerionenforschung mbH
Planckstrasse 1
D-64291 Darmstadt
GERMANY
www.gsi.de



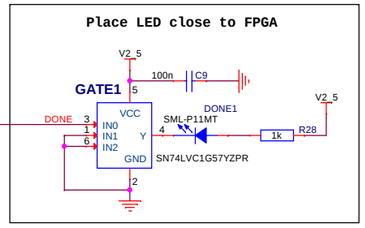


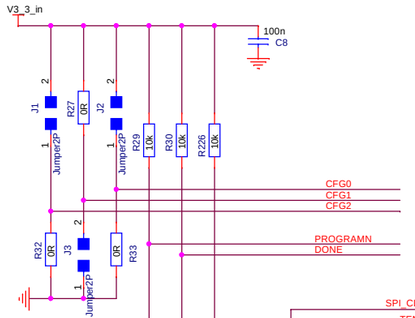
Place JTAG connector close to the edge

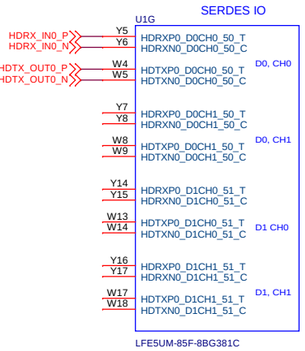


@PETER:
Bitte korrektes Symbol einfügen.

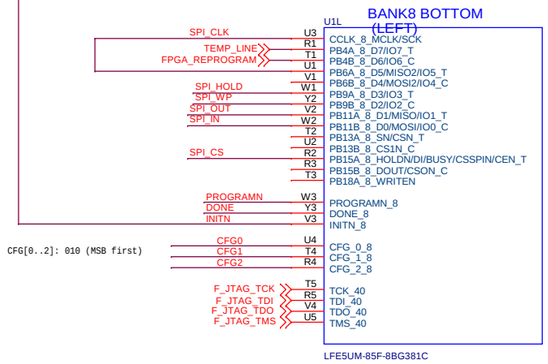
in the final system, light should be off...
So, maybe we remove this LED again...







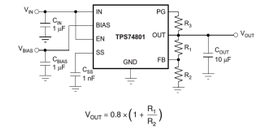
unused serdes channels can be left unpowered and
input signals left floating.
VCCA has always to be powered.

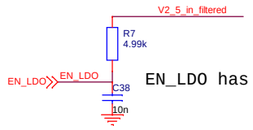


Gesellschaft für Schwerionenforschung mbH
Planckstrasse 1
D-64291 Darmstadt
GERMANY
www.gsi.de

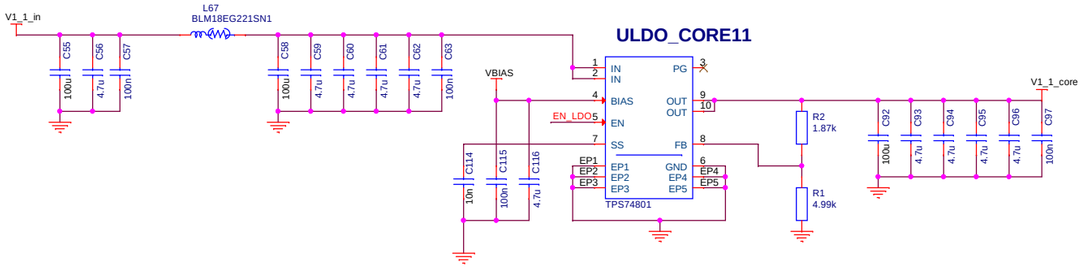
<Title>

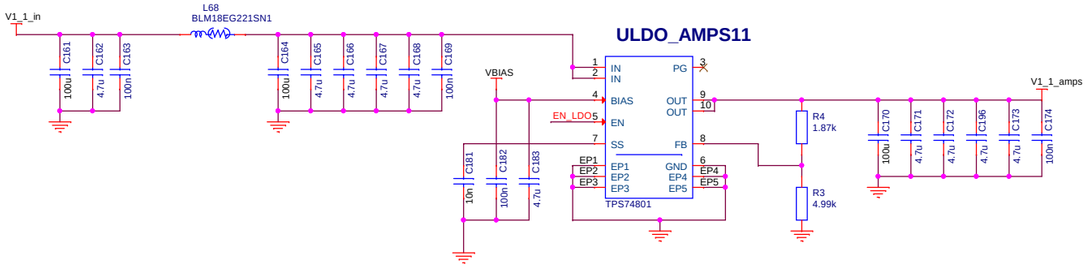
Design: K:\GSI\JOB\COME_AND_KISS\DIRICH\DIRICH1\DIRICH1.DSN
Modified: Tuesday, March 15, 2016
Designer: <Designer>
Size: A2 Page: 3 / 8
Layouter: <Layouter>

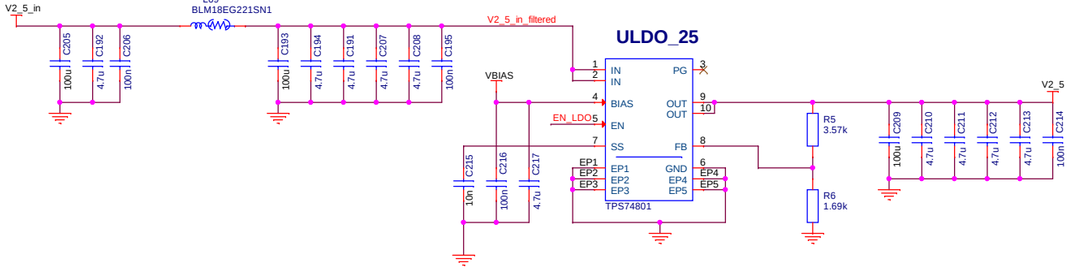


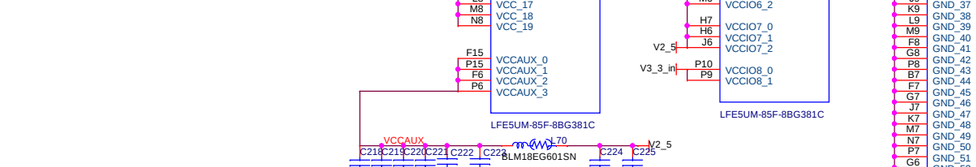


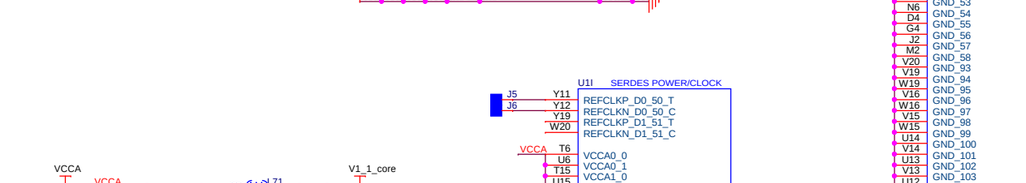
EN_LDO has to be driven above 1.1V to be turned on!



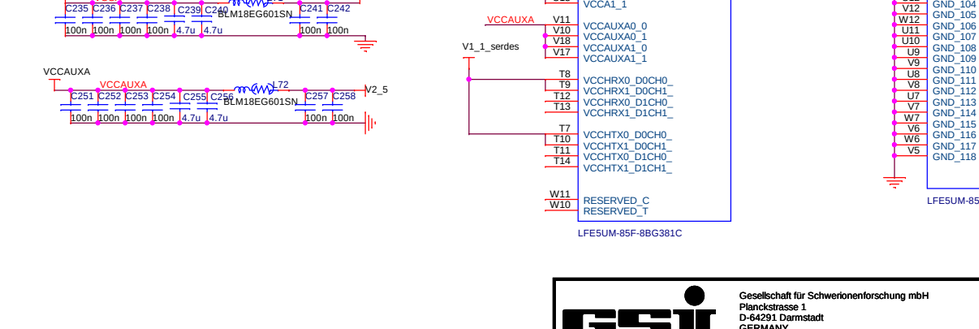


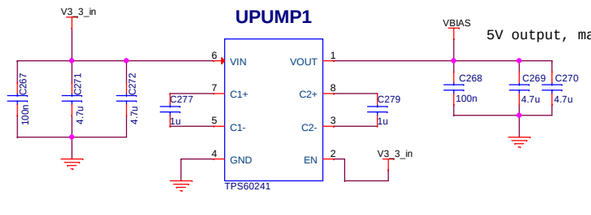






@PETER
die 47nF 0201 sollten durch
33nF 0201 getauscht werden...
GRM033B10J333KE01#
würde es tun.

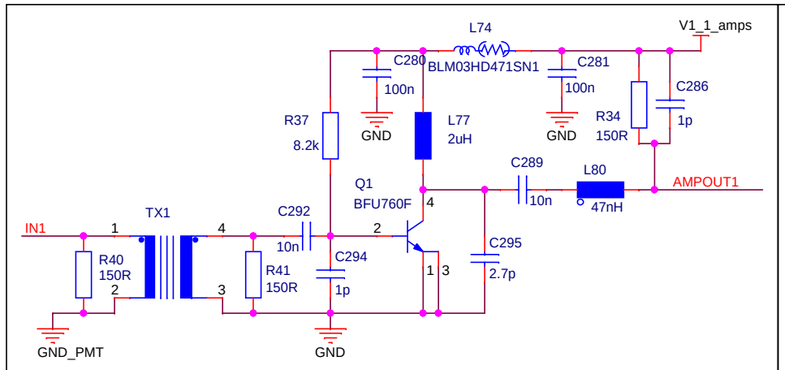


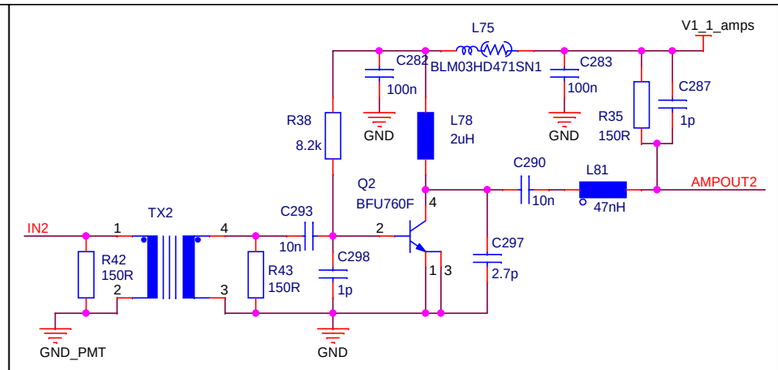


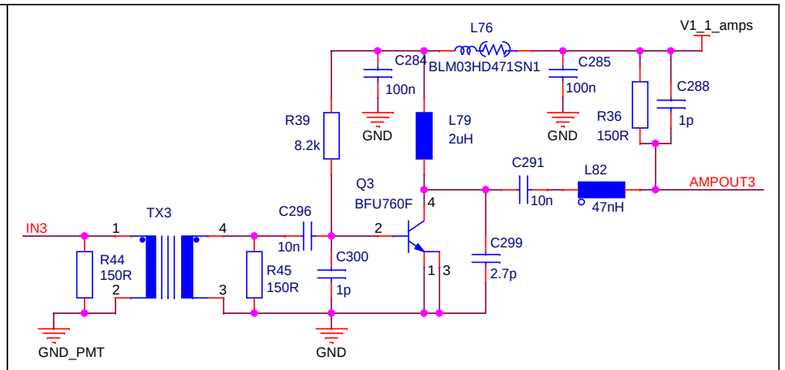
Gesellschaft für Schwerionenforschung mbH
Planckstrasse 1
D-64291 Darmstadt
GERMANY
www.gsi.de

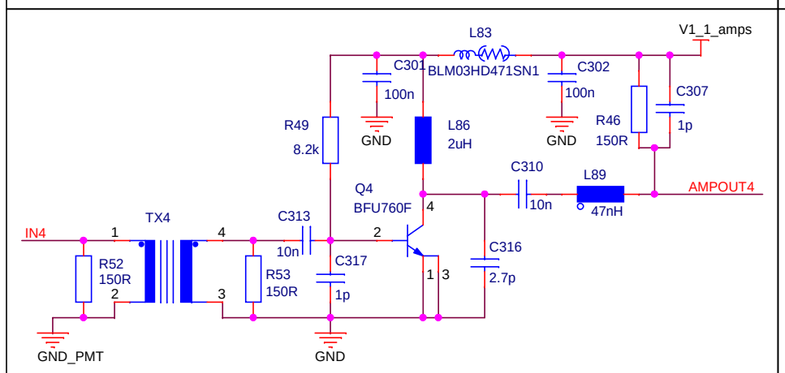
<Title>

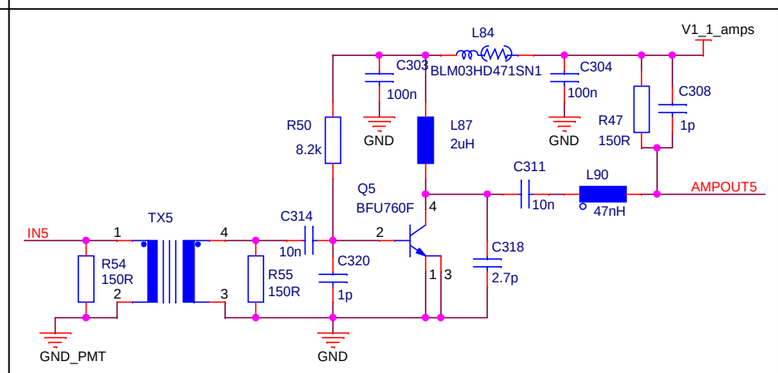
Design: K:\GSI\JOB\COME_AND_KISS\DIRICH\DIRICH1\DIRICH1.DSN
Modified: Tuesday, March 15, 2016
Designer: <Designer>
Size: A2 Page: 4 / 8
Layouter: <Layouter>

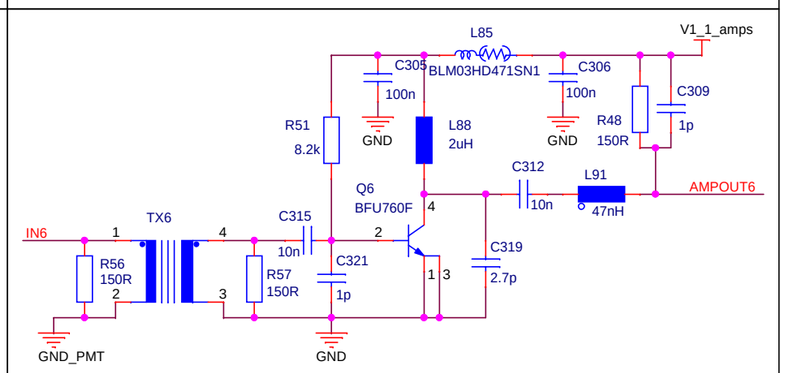


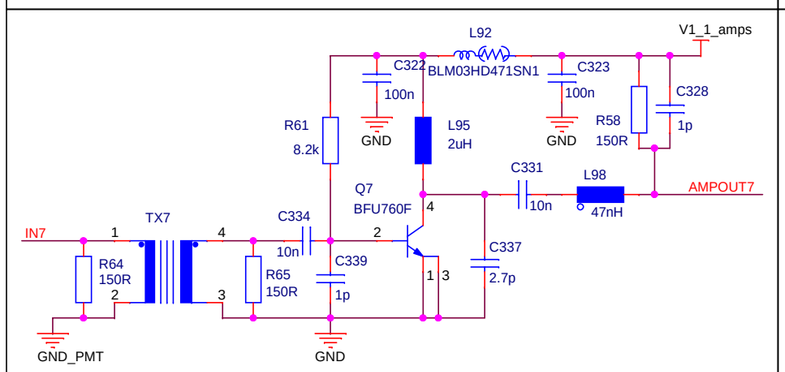


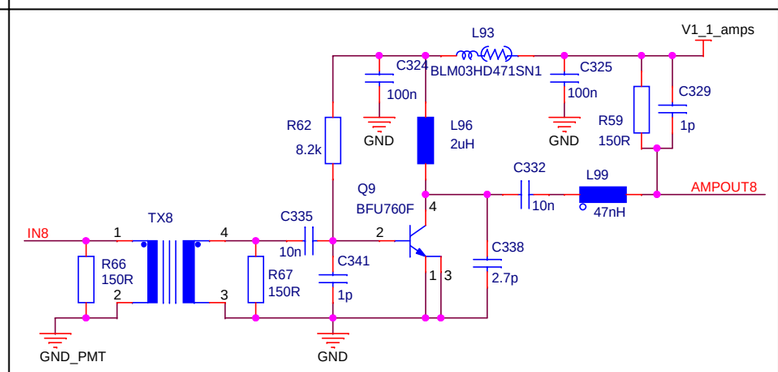


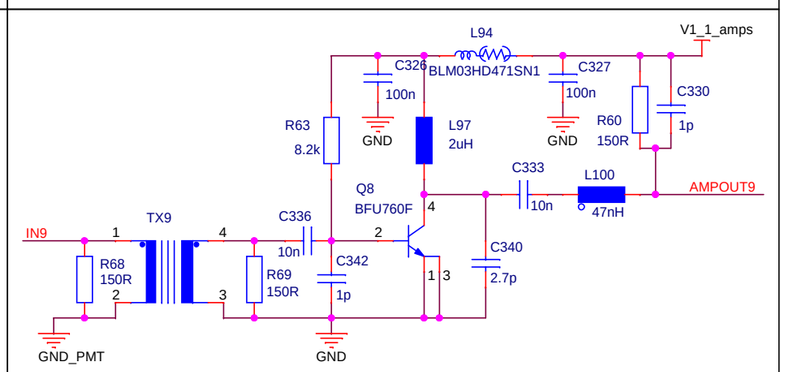


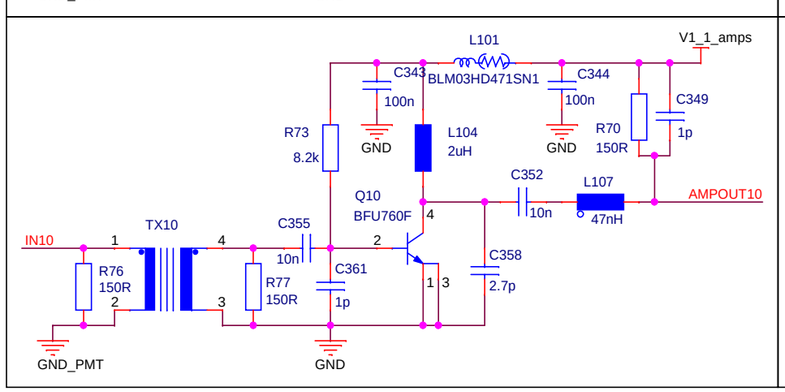


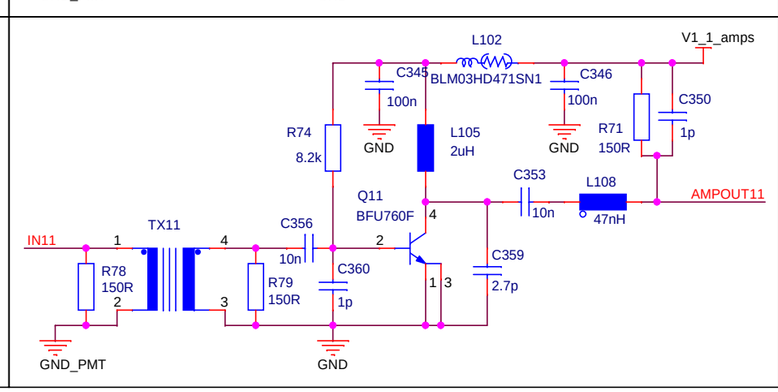


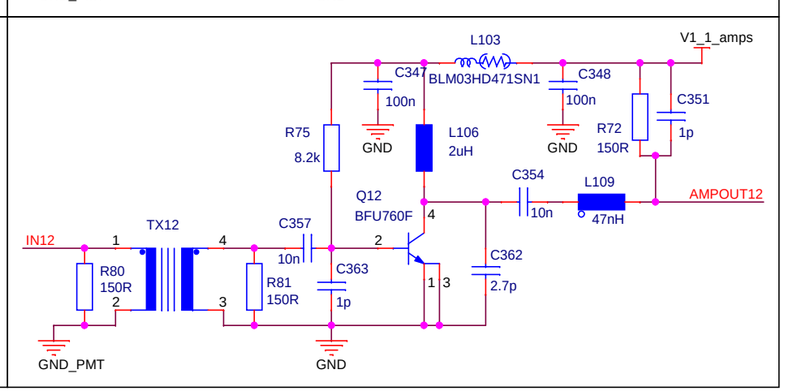












IN[32..1] IN[32..1]

AMPOUT[32..1] AMPOUT[32..1]

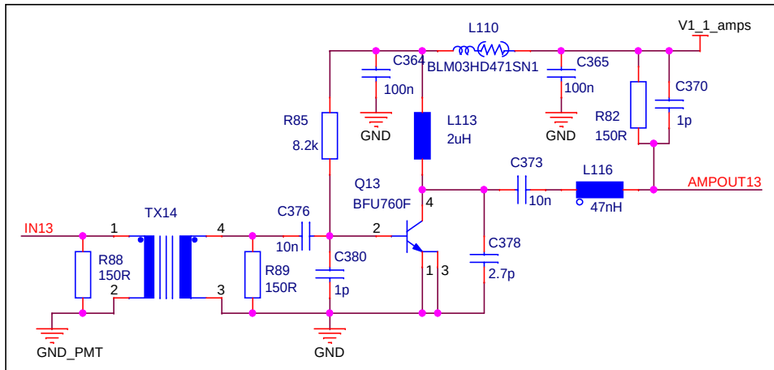
Gesellschaft für Schwerionenforschung mbH
Planckstrasse 1
D-64291 Darmstadt
GERMANY
www.gsi.de

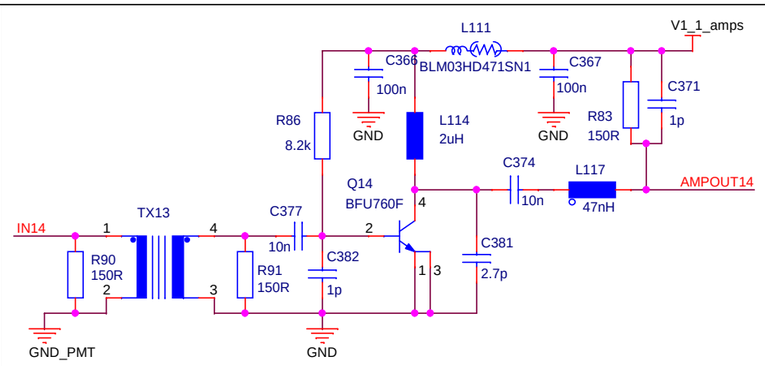
no via for cap,
directly connect E and C
several GND through vias

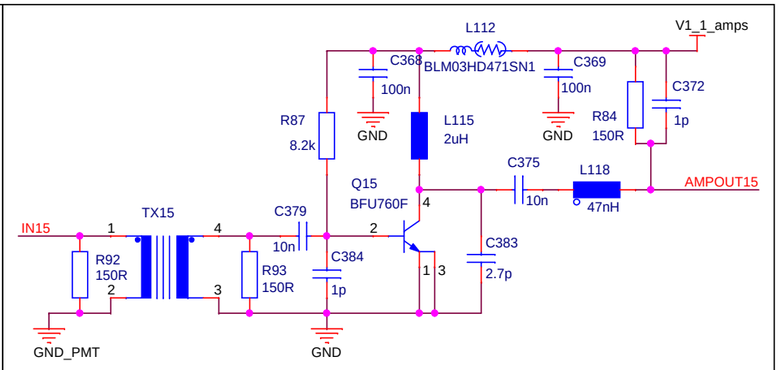
CHANNEL 1-12

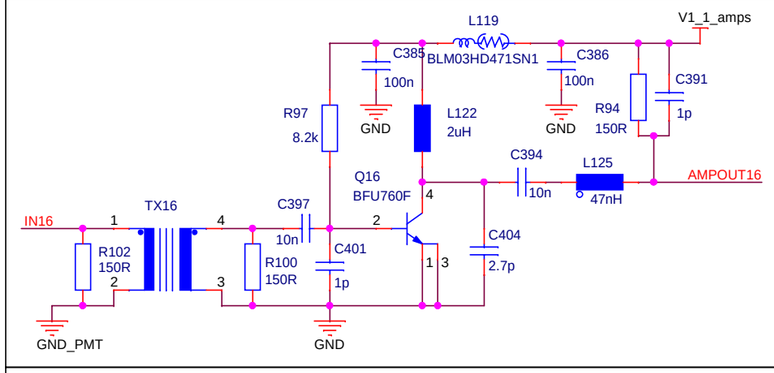
Termination Resistor and
capacitor are near FPGA

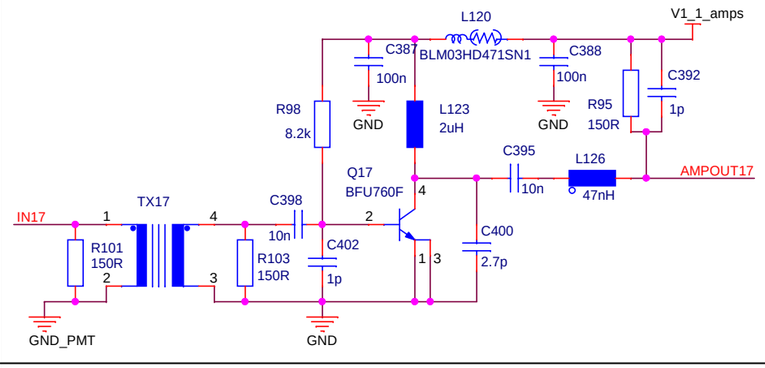
Design: K:\GSIJOB\COME_AND_KISS\DIRICH\DIRICH1\DIRICH1.DSN	
Modified: Tuesday, March 15, 2016	Size: A3 Page: 5 / 8
Designer: <Designer>	Layouter: <Layouter>

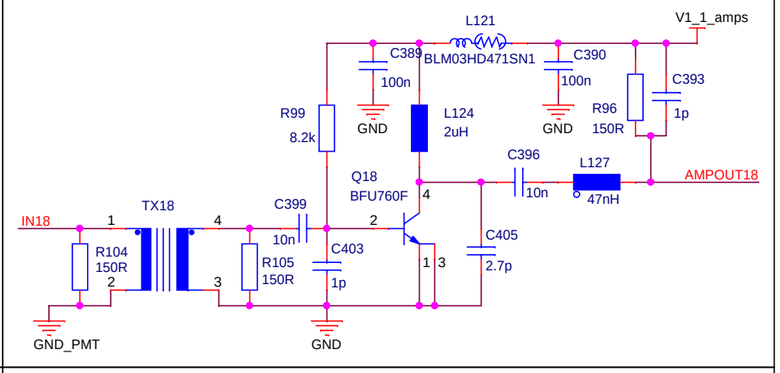


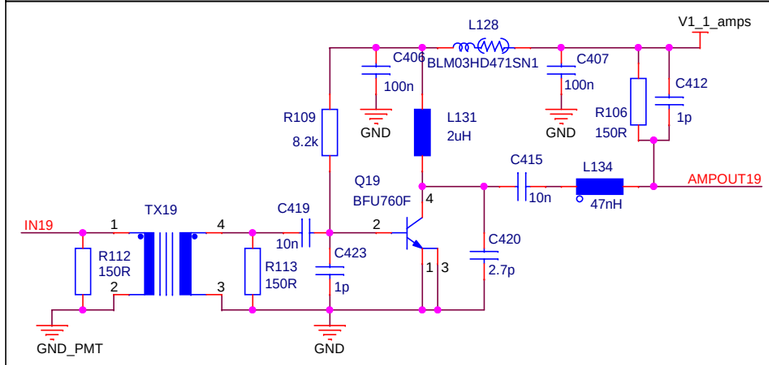


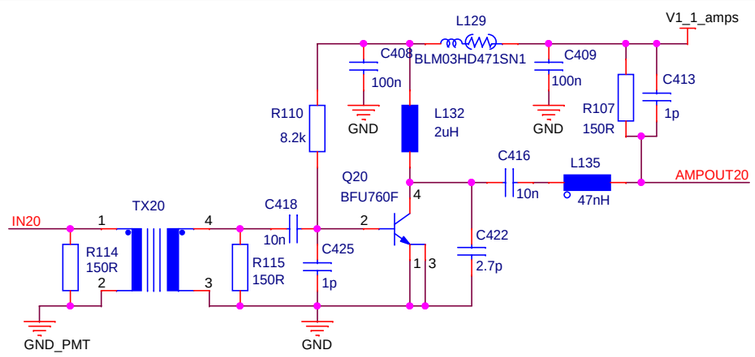


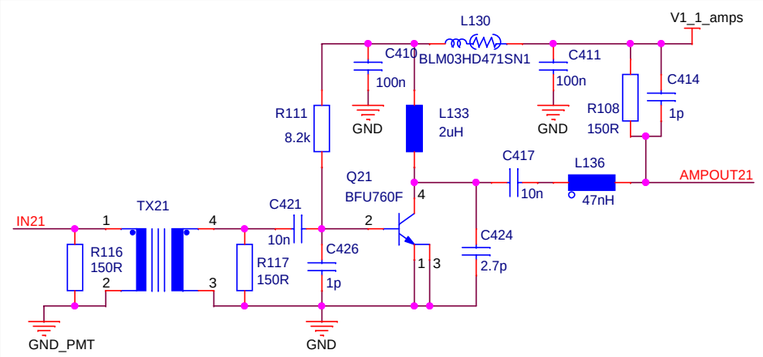


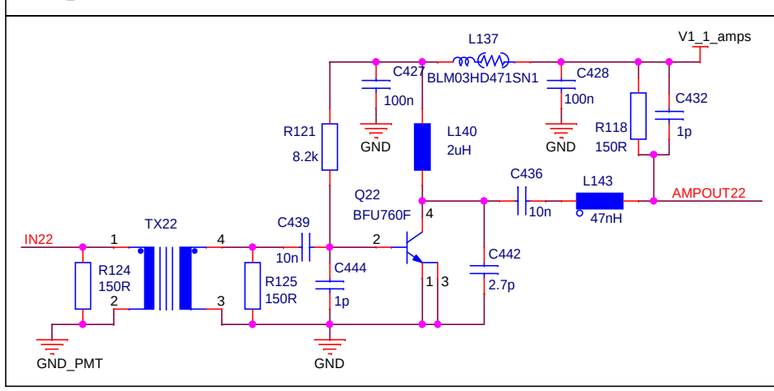


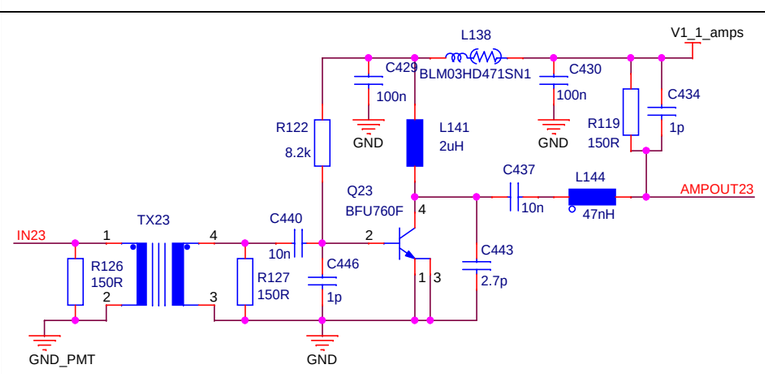


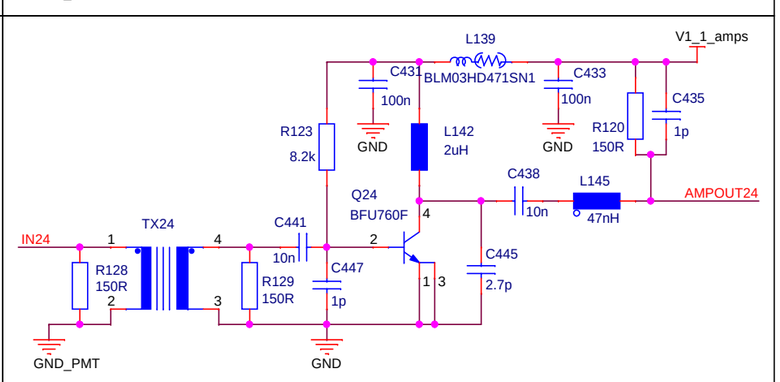












IN[32..1] IN[32..1]

AMPOUT[32..1] AMPOUT[32..1]

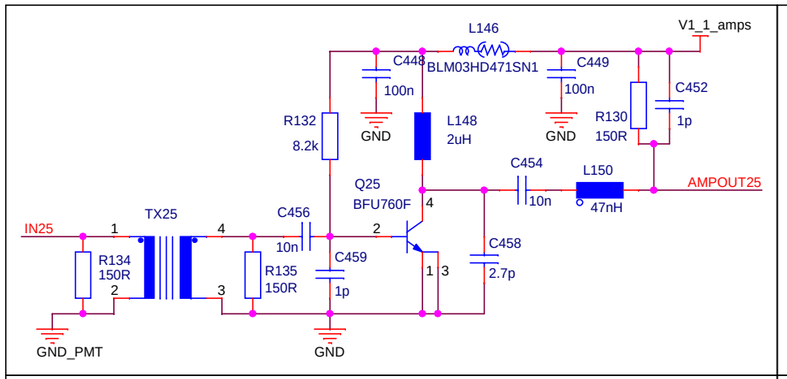
Gesellschaft für Schwerionenforschung mbH
Planckstrasse 1
D-64291 Darmstadt
GERMANY
www.gsi.de

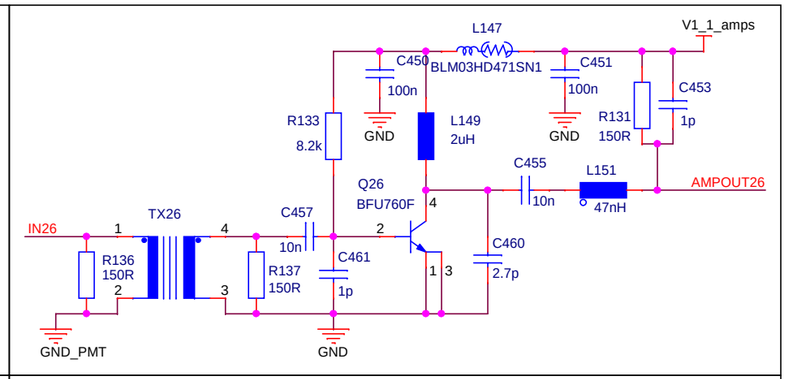
no via for cap,
directly connect E and C
several GND through vias

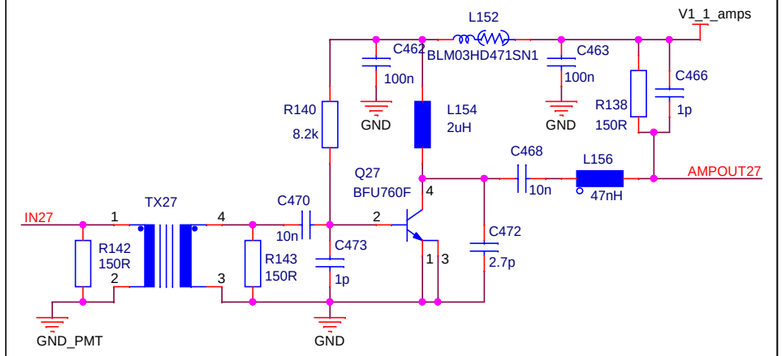
CHANNEL 13-24

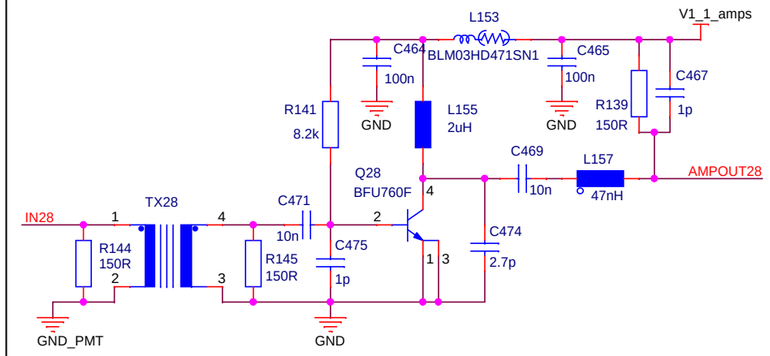
Termination Resistor and
capacitor are near FPGA

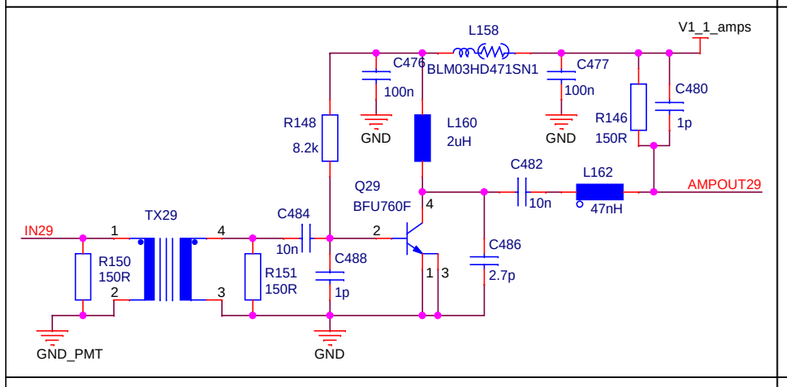
Design: K:\GSIJOB\COME_AND_KISS\DIRICH\DIRICH1\DIRICH1.DSN		
Modified: Tuesday, March 15, 2016	Size: A3	Page: 6 / 8
Designer: <Designer>	Layouter: <Layouter>	

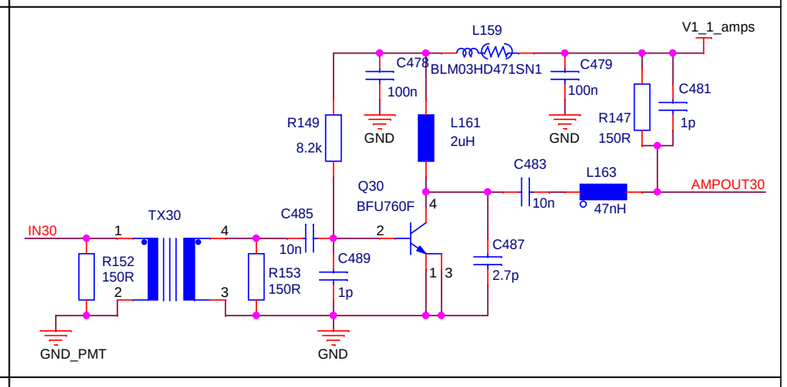


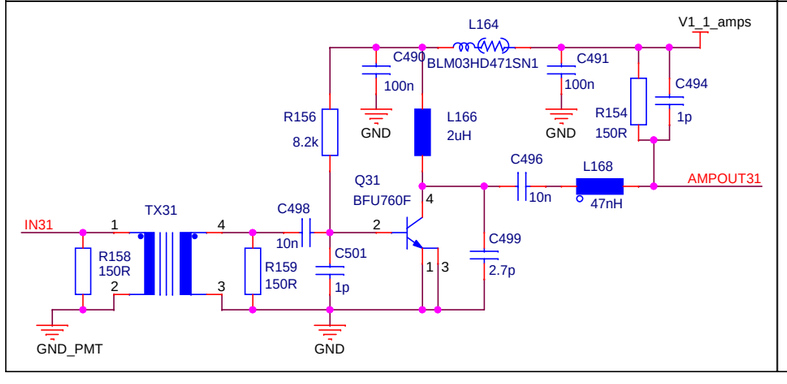


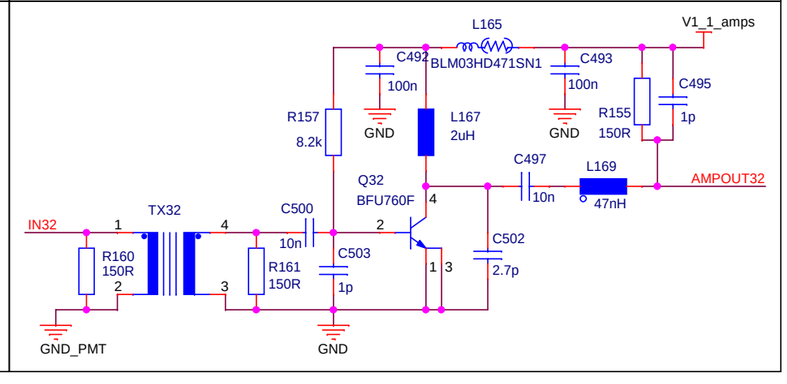












IN[32..1] IN[32..1]

AMPOUT[32..1] AMPOUT[32..1]

Gesellschaft für Schwerionenforschung mbH
Planckstrasse 1
D-64291 Darmstadt
GERMANY
www.gsi.de

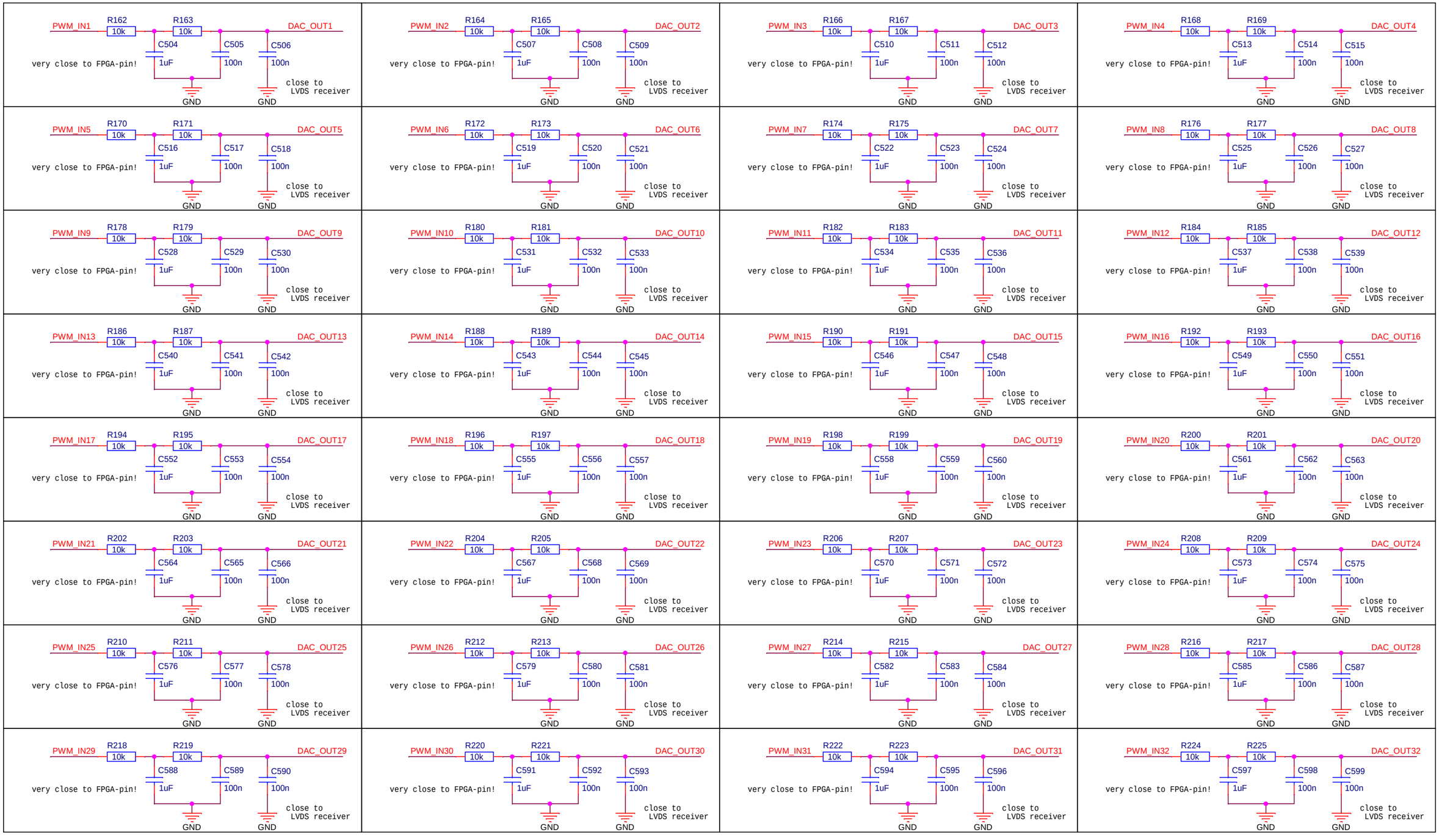
no via for cap,
directly connect E and C
several GND through vias

CHANNEL 25-32

Termination Resistor and
capacitor are near FPGA

Design:	K:\GSIJOB\COME_AND_KISS\DIRICH\DIRICH1\DIRICH1.DSN	
Modified:	Tuesday, March 15, 2016	Size: A3 Page: 7 / 8
Designer:	<Designer>	Layouter: <Layouter>

wire around FPGA, from output side to input side



PWM_IN[32..1] PWM_IN[32..1]

DAC_OUT[32..1] DAC_OUT[32..1]

Gesellschaft für Schwerionenforschung mbH
Planckstrasse 1
D-64291 Darmstadt
GERMANY
www.gsi.de

DACs_1-16

Design: K:\GSIJOB\COME_AND_KISS\DIRICH\DIRICH1\DIRICH1.DSN	
Modified: Tuesday, March 15, 2016	Size: A3 Page: 8 / 8
Designer: <Designer>	Layouter: <Layouter>