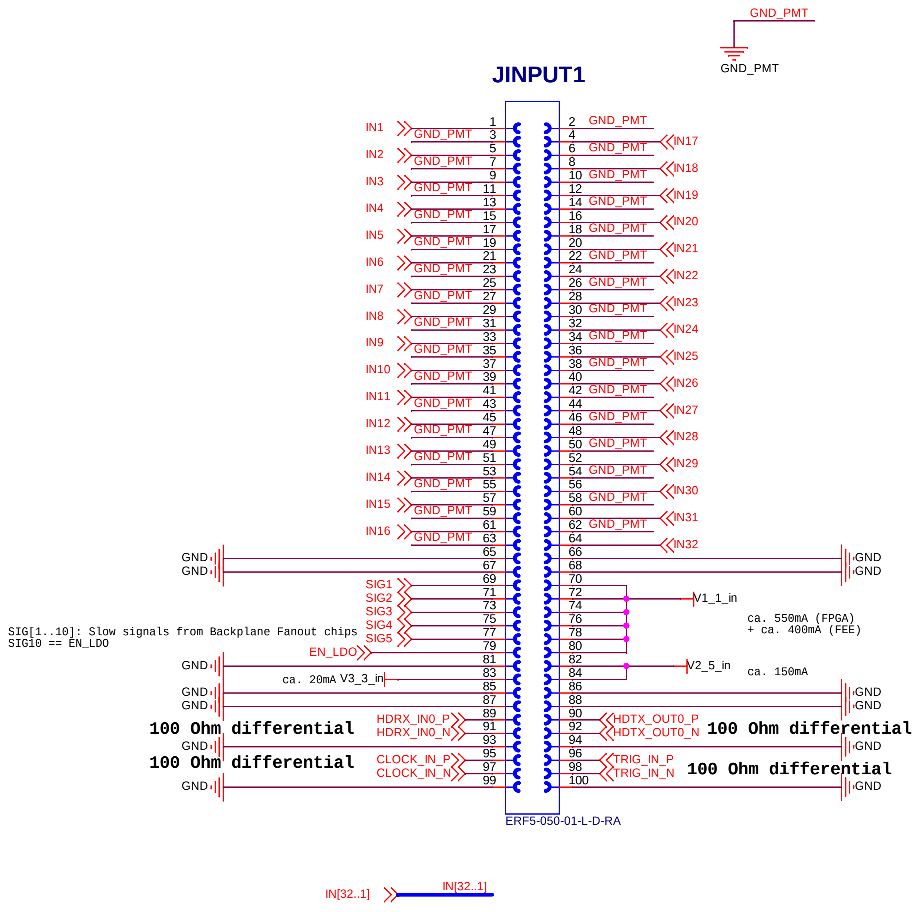
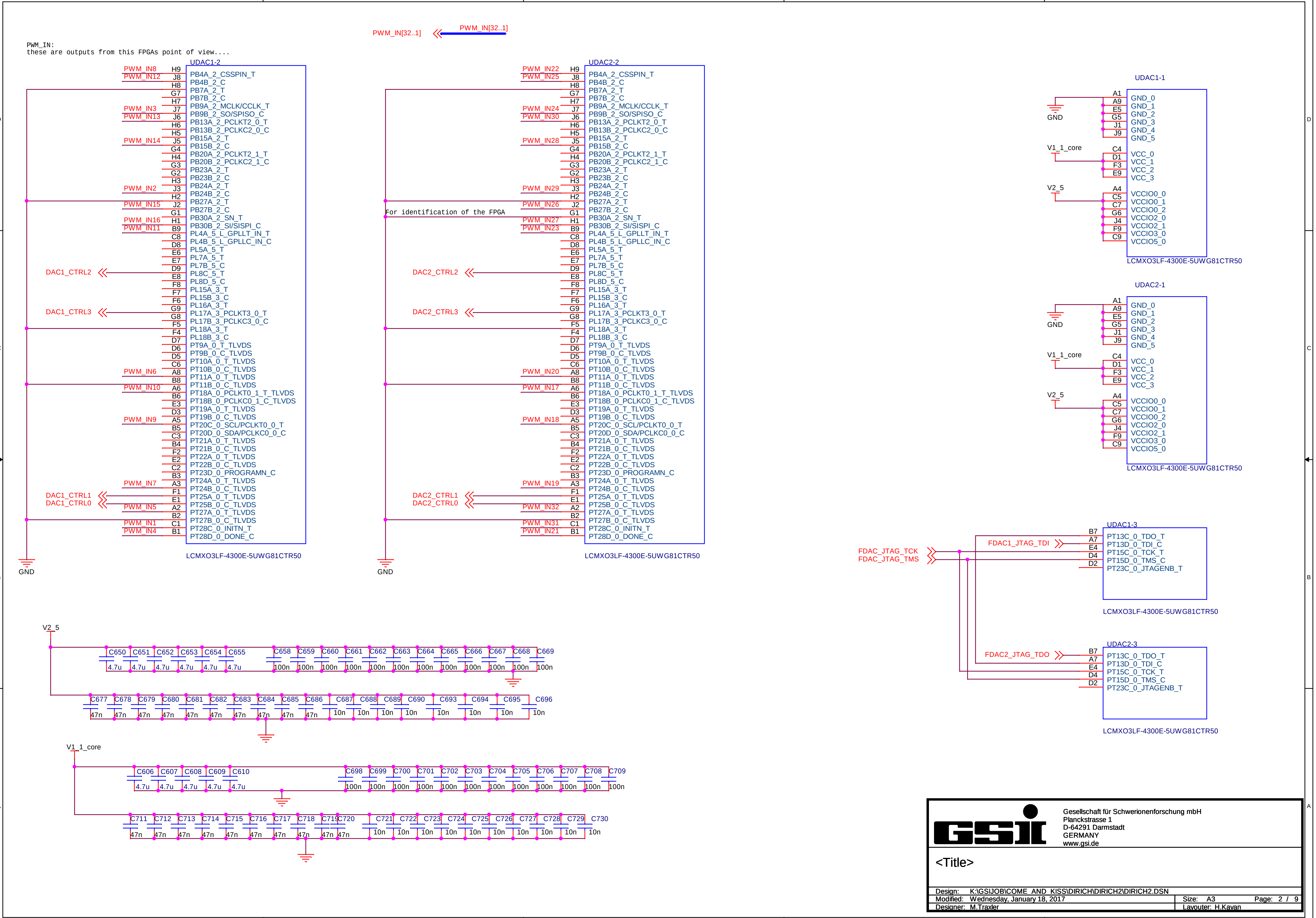


Gesellschaft für Schwerionenforschung mbH
Plancksstrasse 1
D-64291 Darmstadt
GERMANY
www.gsi.de

<Title>

Design: K:\GSIJOB\COME_AND_KISS\DIRICH\DIRICH2\DIRICH2.DSN
Modified: Wednesday, January 18, 2017
Designer: M.Traxler
Size: A3
Layouter: H.Kayan
Page: 1 / 9

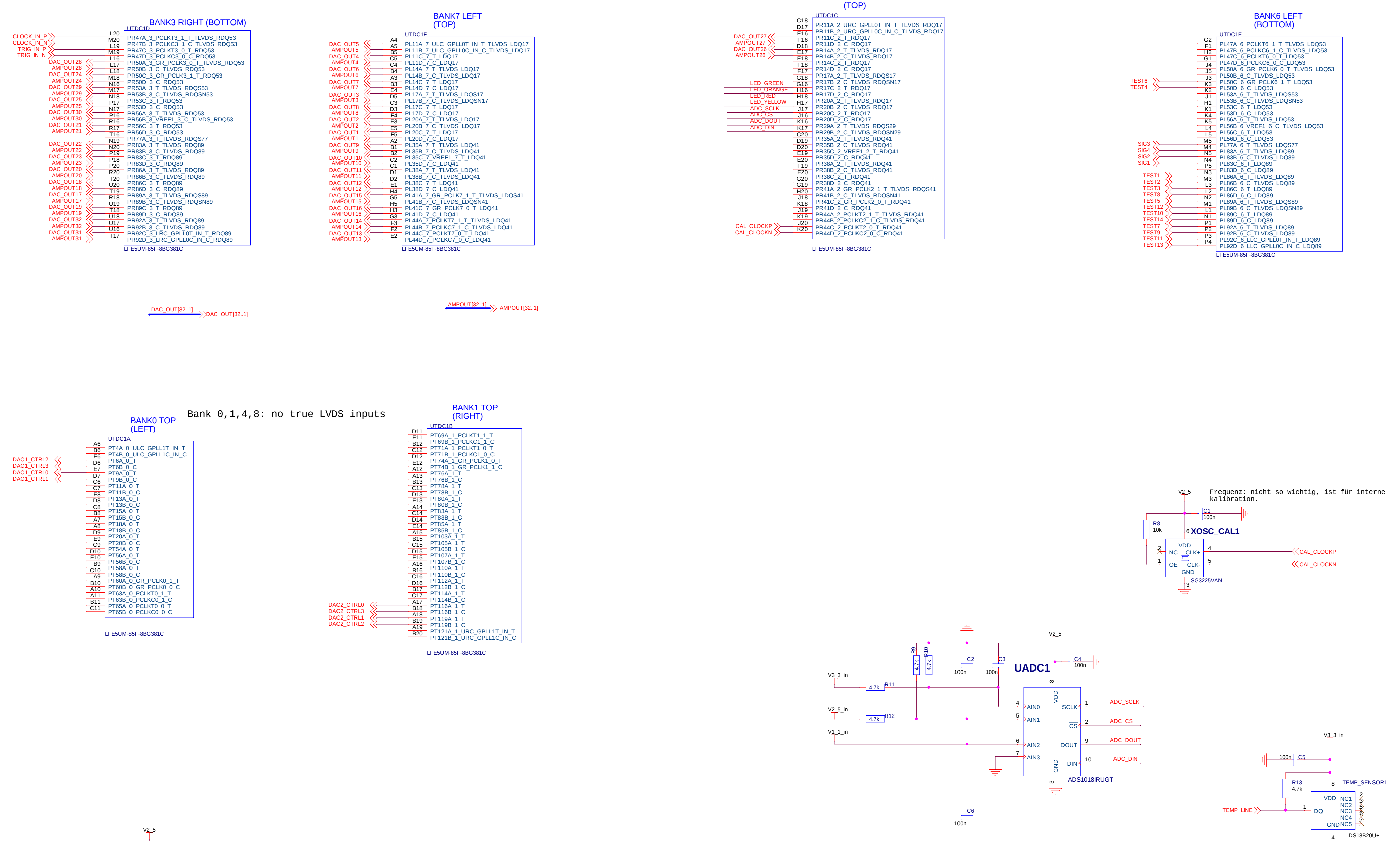


Gesellschaft für Schwerionenforschung mbH
Planckstrasse 1
D-64291 Darmstadt
GERMANY
www.gsi.de

<Title>

Design: K:\GSIJOB\COME_AND_KISS\DIRICH\DIRICH2\DIRICH2.DSN
Modified: Wednesday, January 18, 2017 | Size: A3 | Page: 2 / 9
Designer: M.Traxler | Layouter: H.Kayan

Bank 0,1,4,8: no true LVDS inputs
Bank 2,3,6,7: LVDS inputs, 50% LVDS outputs

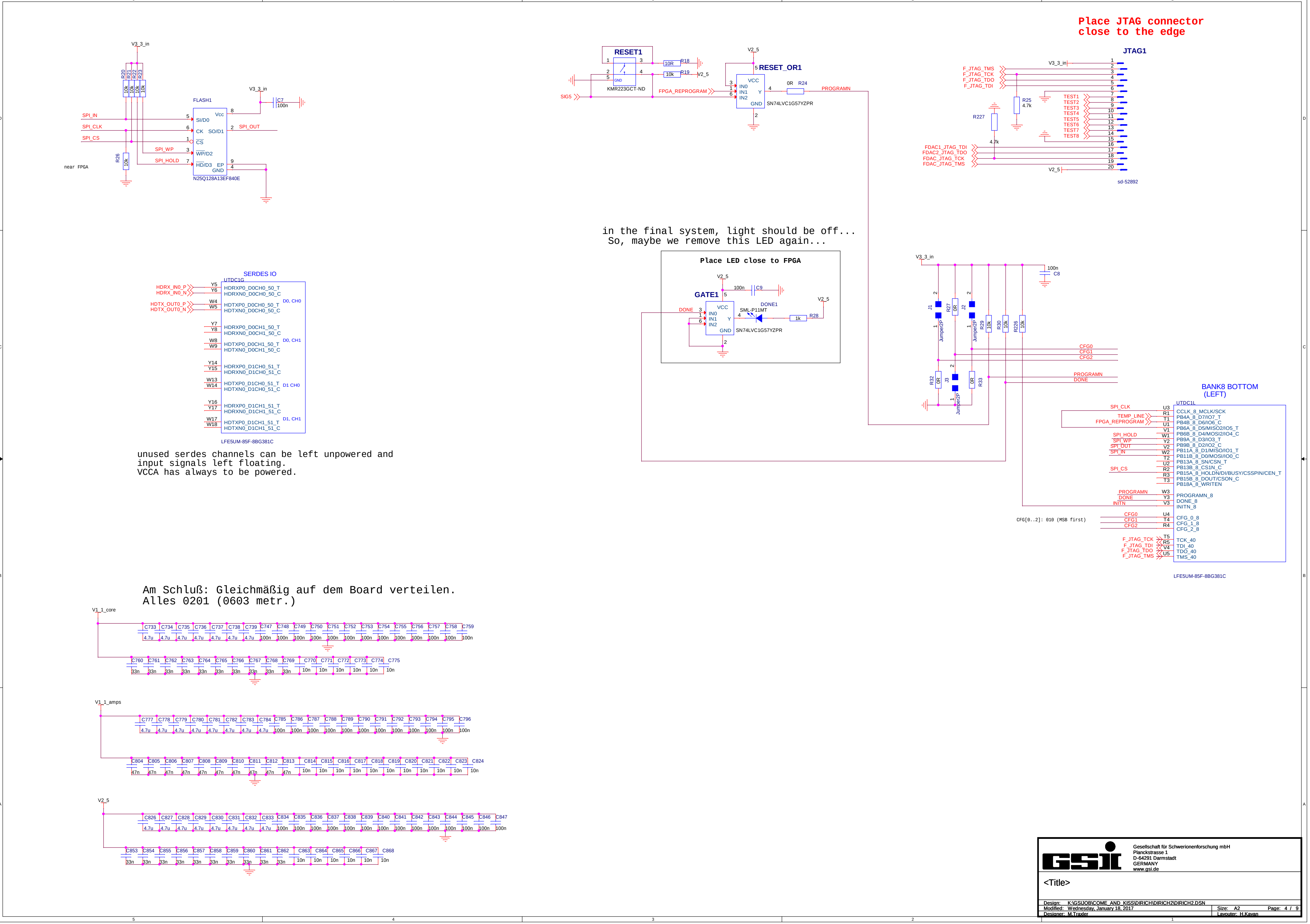


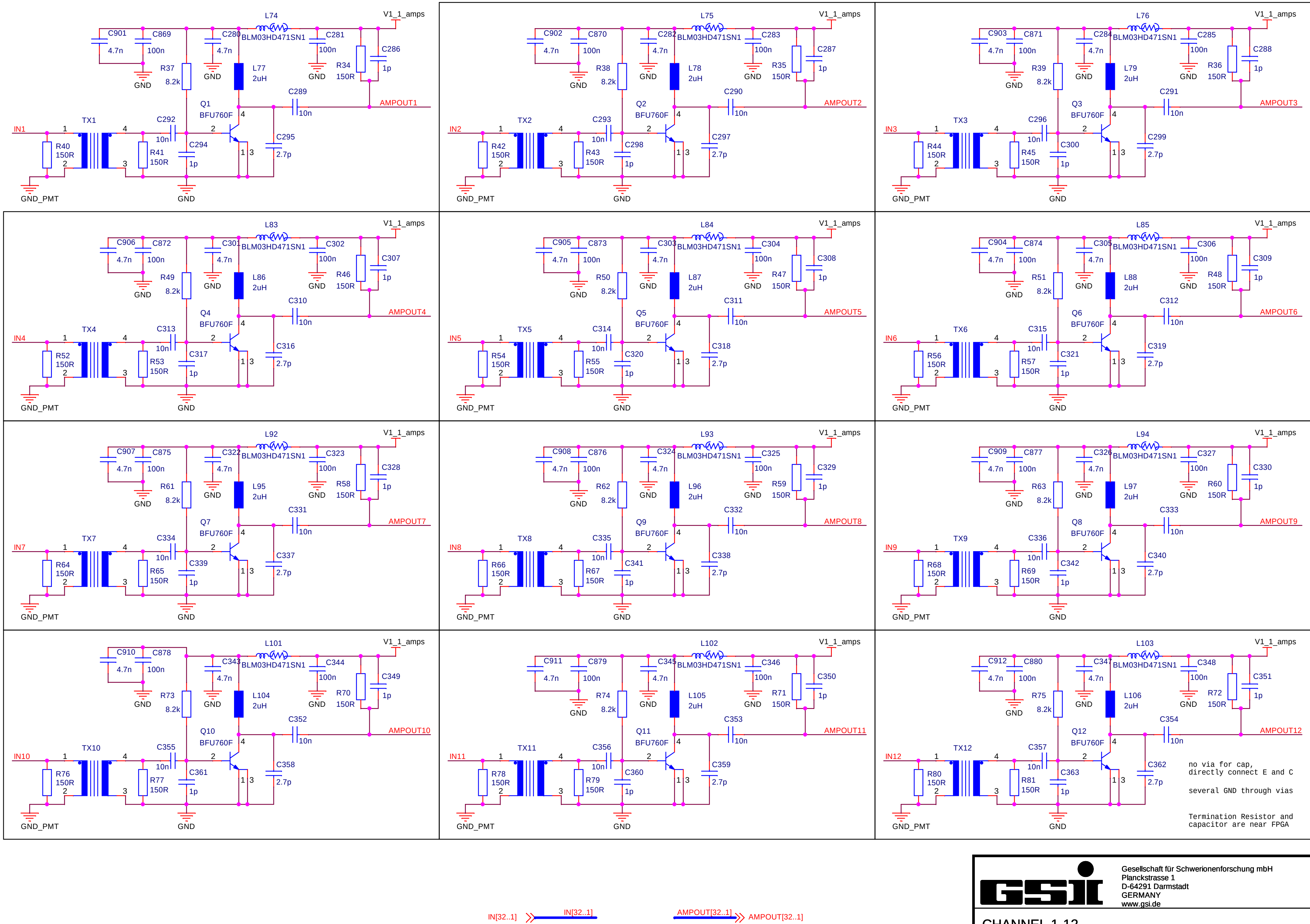
Part No.	Resin Color	Forward voltage V_F		Reverse current I_R		Light wavelength Dominant λD		Brightness I_V		
		Typ. (V)	I_F (mA)	Max. (µA)	V_R (V)	Typ. (nm)	I_F (mA)	Min. (mcd)	Typ. (mcd)	I_F (mA)
SML-P11MT	Transparent Colorless	1.9	1	100	4	569	1	0.63	2.1	1
SML-P11YT		1.9				586		2.5	7.6	
SML-P11DT		1.8				605		2.5	7.3	
SML-P11UT		1.8				621		1.6	5.5	
SML-P11VT		1.8				626		1.0	3.6	

Gesellschaft für Schwerionenforschung mbH
Planckstrasse 1
D-64291 Darmstadt
GERMANY
www.gsi.de

<Title>

Design: K:\GSIJOB\COME_AND_KISS\DIRICH\DIRICH2\DIRICH2.DSN
Modified: Wednesday, January 18, 2017 | Size: A2 | Page: 3 / 9
Designer: M.Traxler | Layouter: H.Kavan

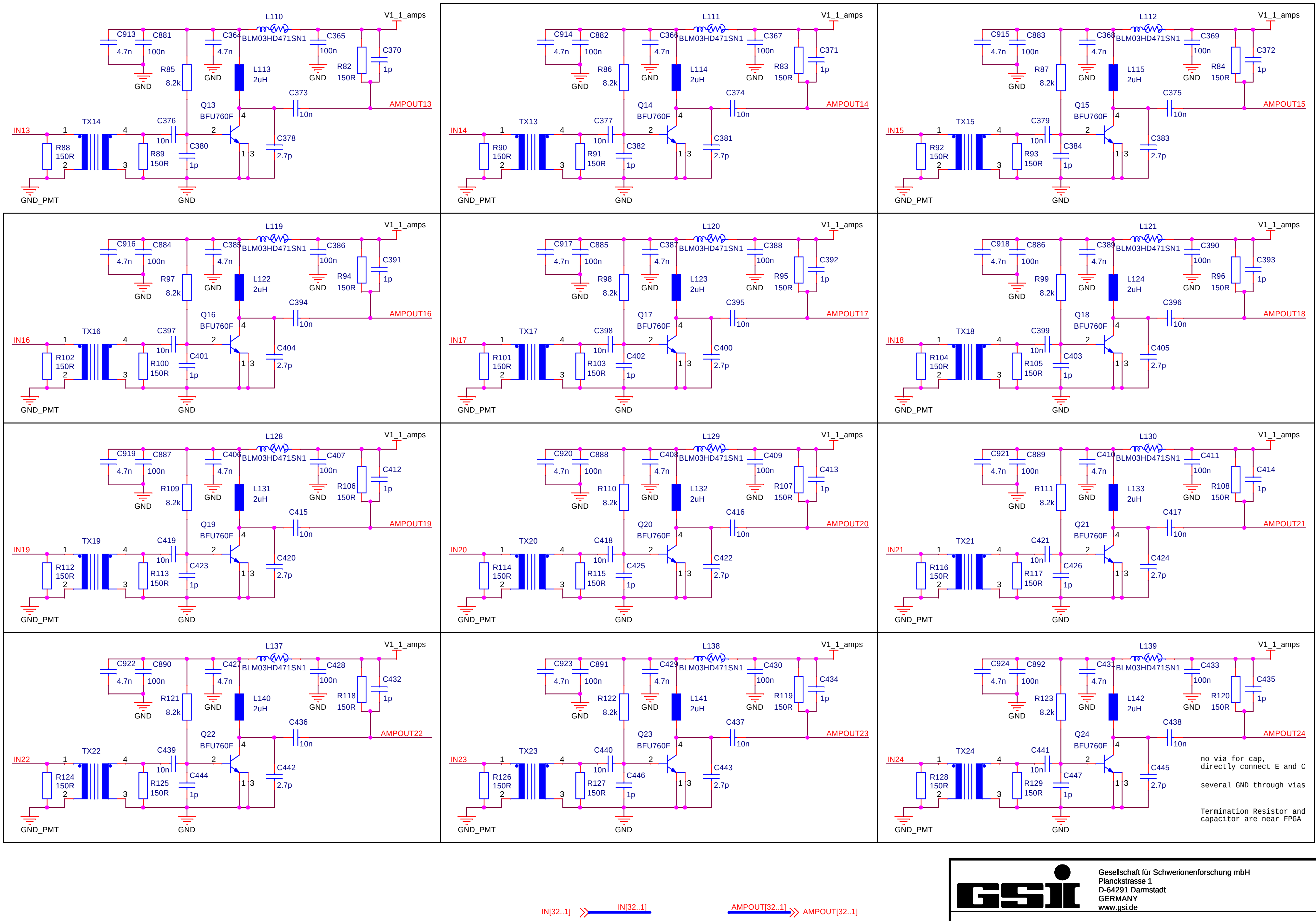

Place JTAG connector close to the edge
JTAG1
sd-52892
RESET1
KMR223GCT-ND
RESET_OR1
SN74LVC1G57YZPR
PROGRAMN
FPGA_REPROGRAM
SIG5
FLASH1
N25Q128A13EF840E
near FPGA
SPI_IN
SPI_CLK
SPI_CS
SPI_WP
SPI_HOLD
SPI_OUT
in the final system, light should be off...
So, maybe we remove this LED again...
Place LED close to FPGA
GATE1
SN74LVC1G57YZPR
DONE1
SML-P11MT
SERDES IO
LFE5UM-85F-8BG381C
unused serdes channels can be left unpowered and
input signals left floating.
VCCA has always to be powered.
BANK8 BOTTOM
(LEFT)
CFG[0..2]: 010 (MSB first)
LFE5UM-85F-8BG381C
Am Schluß: Gleichmäßig auf dem Board verteilen.
Alles 0201 (0603 metr.)
V1_1_core
V1_1_amps
V2_5
Gesellschaft für Schwerionenforschung mbH
Planckstrasse 1
D-64291 Darmstadt
GERMANY
www.gsi.de
<Title>
Design: K:\GSI\JOB\COME_AND_KISS\DIRICH\DIRICH2\DIRICH2.DSN
Modified: Wednesday, January 18, 2017
Designer: M.Traxler
Size: A2
Page: 4 / 9
Layouter: H.Kavan



Gesellschaft für Schwerionenforschung mbH
Planckstrasse 1
D-64291 Darmstadt
GERMANY
www.gsi.de

CHANNEL 1-12

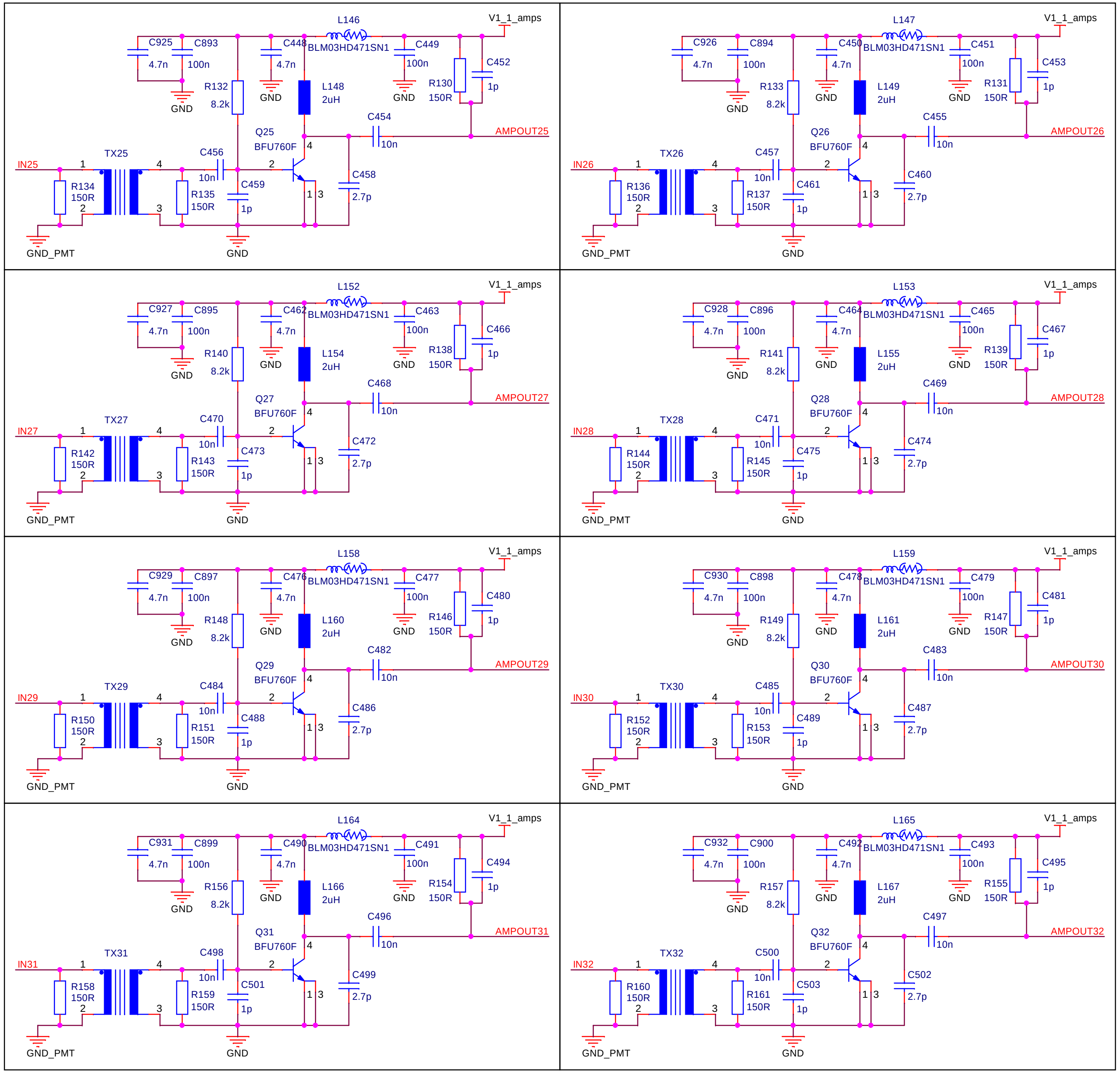
Design: K:\GSIJOB\COME_AND_KISS\DIRICH\DIRICH2\DIRICH2.DSN
Modified: Wednesday, January 18, 2017
Designer: M.Traxler
Size: A3
Layouter: H.Kayan
Page: 5 / 9



Gesellschaft für Schwerionenforschung mbH
Planckstrasse 1
D-64291 Darmstadt
GERMANY
www.gsi.de

CHANNEL 13-24

Design: K:\GSIJOB\COME_AND_KISS\DIRICH\DIRICH2\DIRICH2.DSN
Modified: Wednesday, January 18, 2017
Designer: <Designer>
Size: A3
Layouter: <Layouter>
Page: 6 / 9



IN[32..1] IN[32..1]

AMPOUT[32..1] AMPOUT[32..1]

no via for cap,
directly connect E and C

several GND through vias

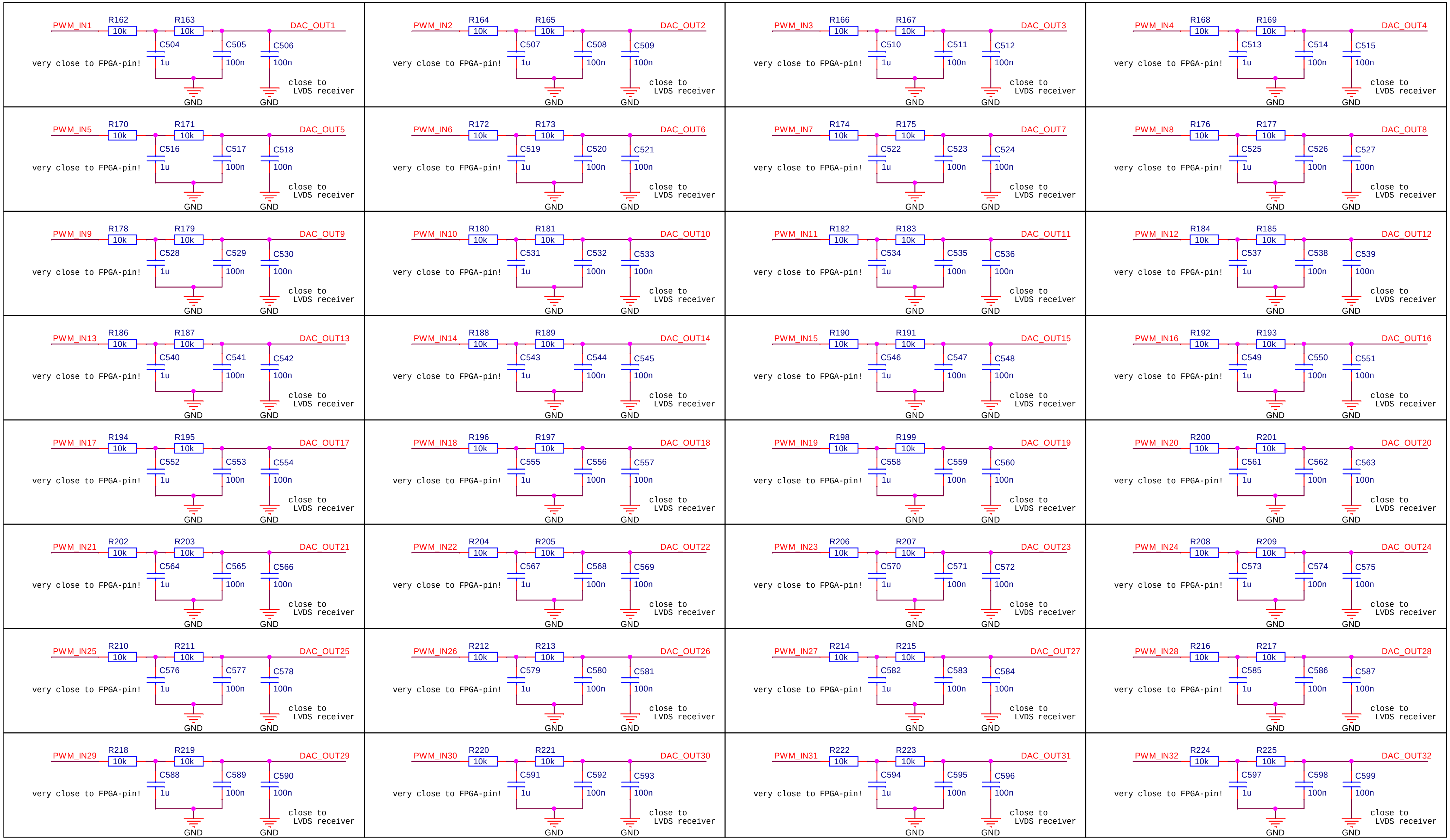
Termination Resistor and
capacitor are near FPGA

Gesellschaft für Schwerionenforschung mbH
Planckstrasse 1
D-64291 Darmstadt
GERMANY
www.gsi.de

CHANNEL 25-32

Design: K:\GSIJOB\COME_AND_KISS\DIRICH\DIRICH2\DIRICH2.DSN
Modified: Wednesday, January 18, 2017
Designer: M.Traxler
Size: A3
Layouter: H.Kayan
Page: 7 / 9

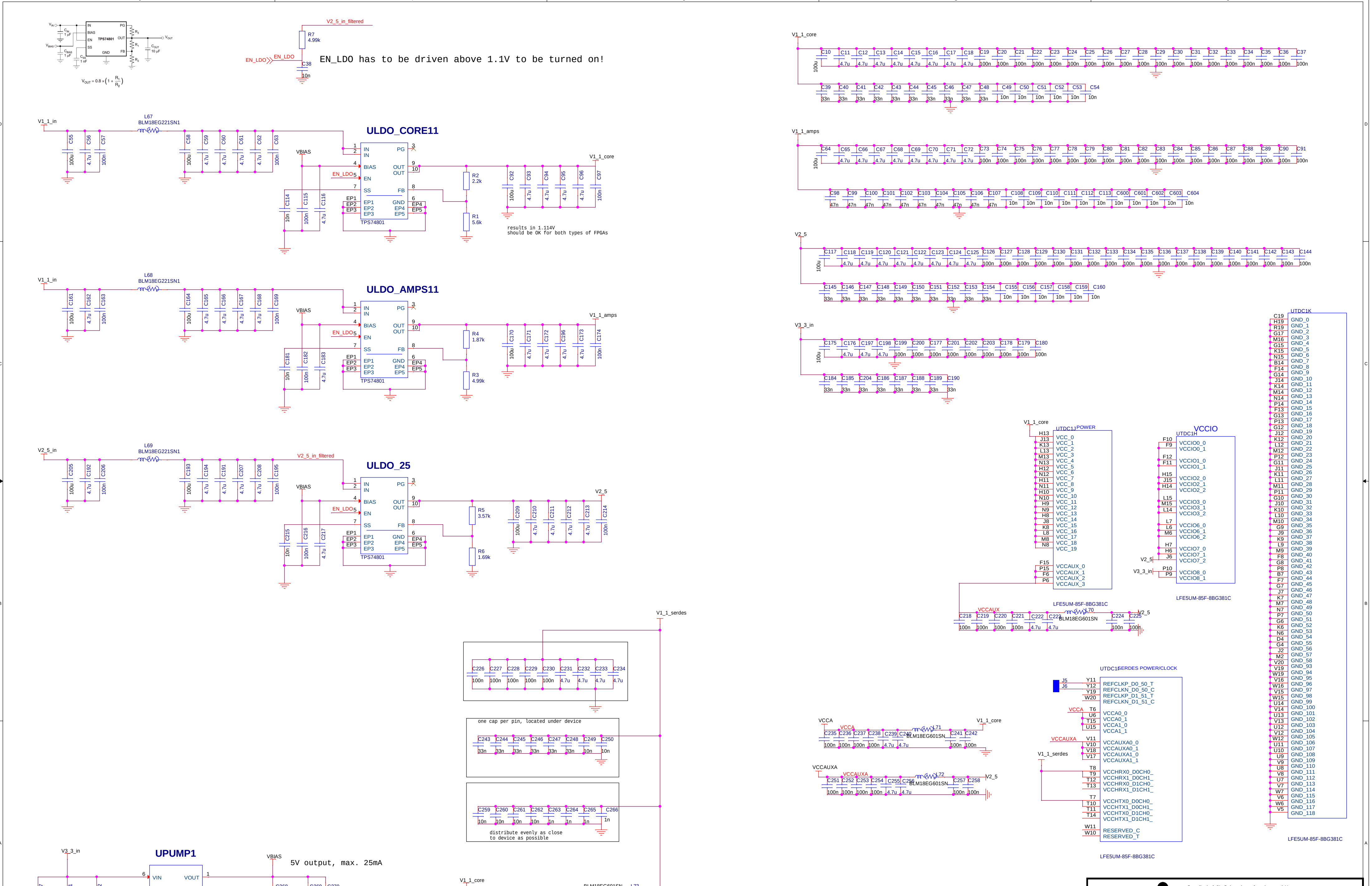
wire around FPGA, from output side to input side



Gesellschaft für Schwerionenforschung mbH
Planckstrasse 1
D-64291 Darmstadt
GERMANY
www.gsi.de

DACs_1-16

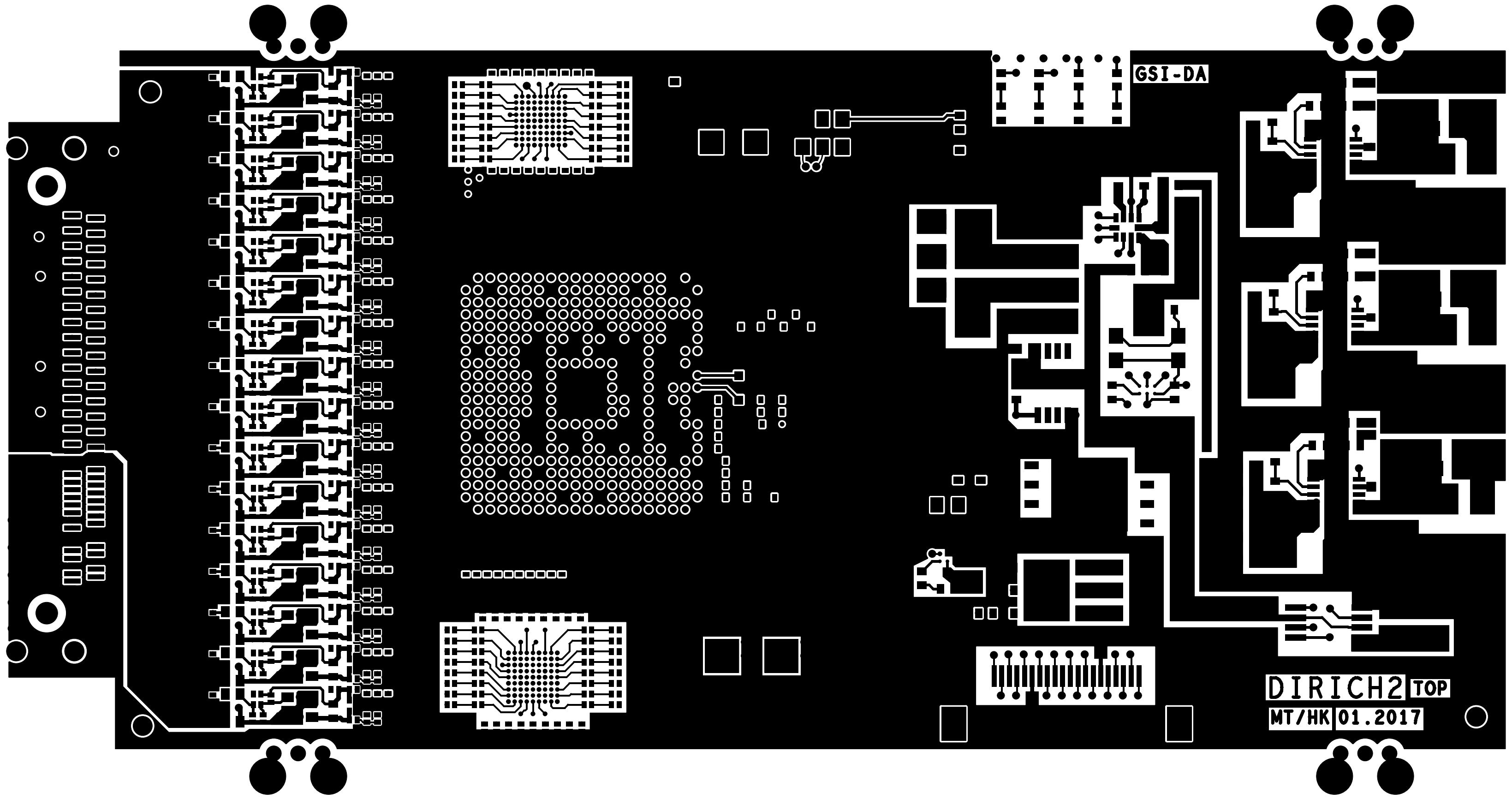
Design: K:\GSIJOB\COME_AND_KISS\DIRICH\DIRICH2\DIRICH2.DSN
Modified: Wednesday, January 18, 2017 | Size: A3 | Page: 8 / 9
Designer: M.Traxler | Layouter: H.Kayan



Gesellschaft für Schwerionenforschung mbH
Planckstrasse 1
D-64291 Darmstadt
GERMANY
www.gsi.de

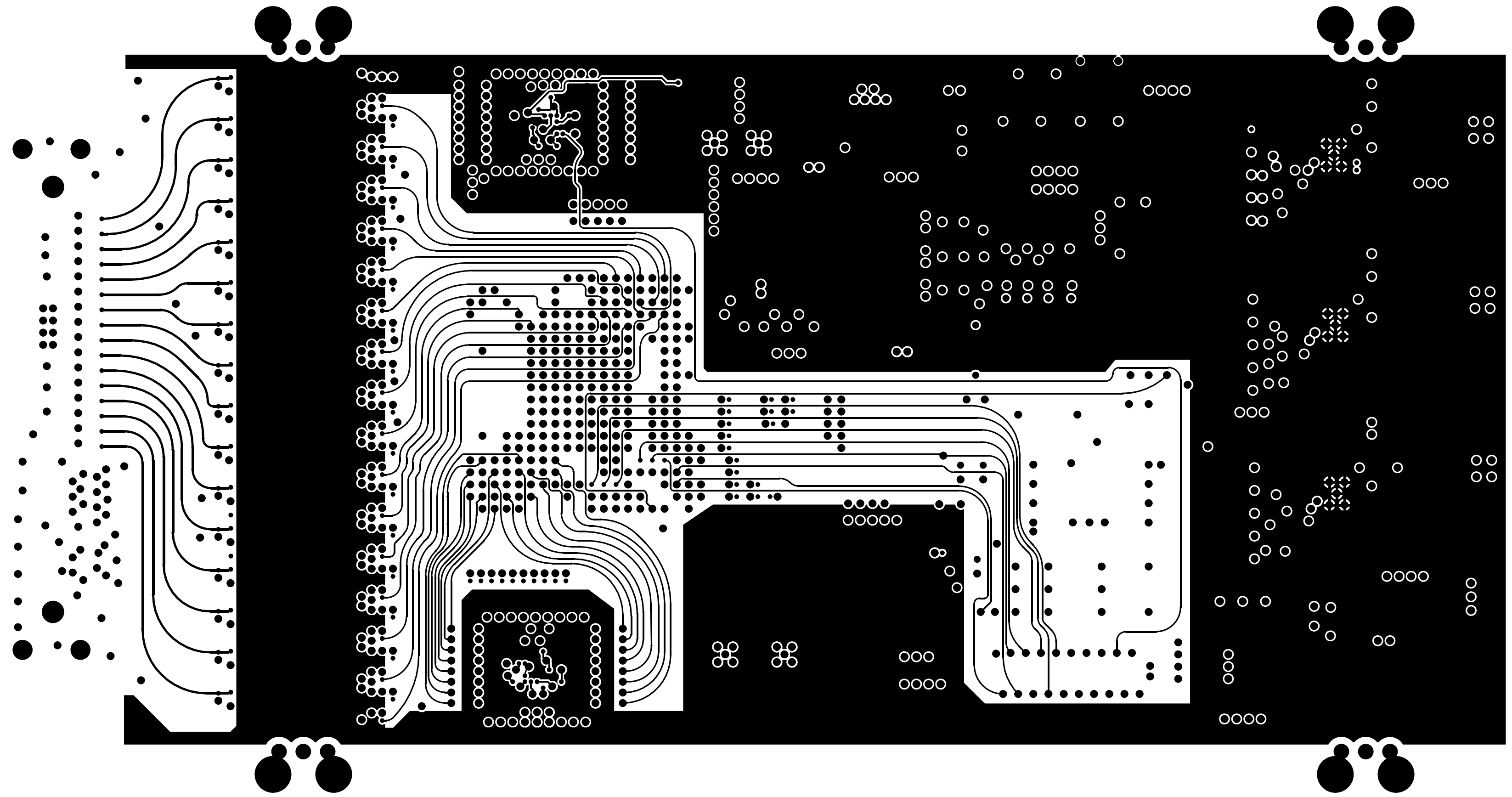
<Title>

Design: K:\GSI\JOB\COME_AND_KISS\DIRICH\DIRICH2\DIRICH2.DSN
Modified: Wednesday, January 18, 2017
Designer: M.Traxler
Size: A2
Page: 9 / 9
Layouter: H.Kavan



Jobname	Date	Designer	Layouter
DIRICH2	01.2017	M.Traxler	H.Kayan

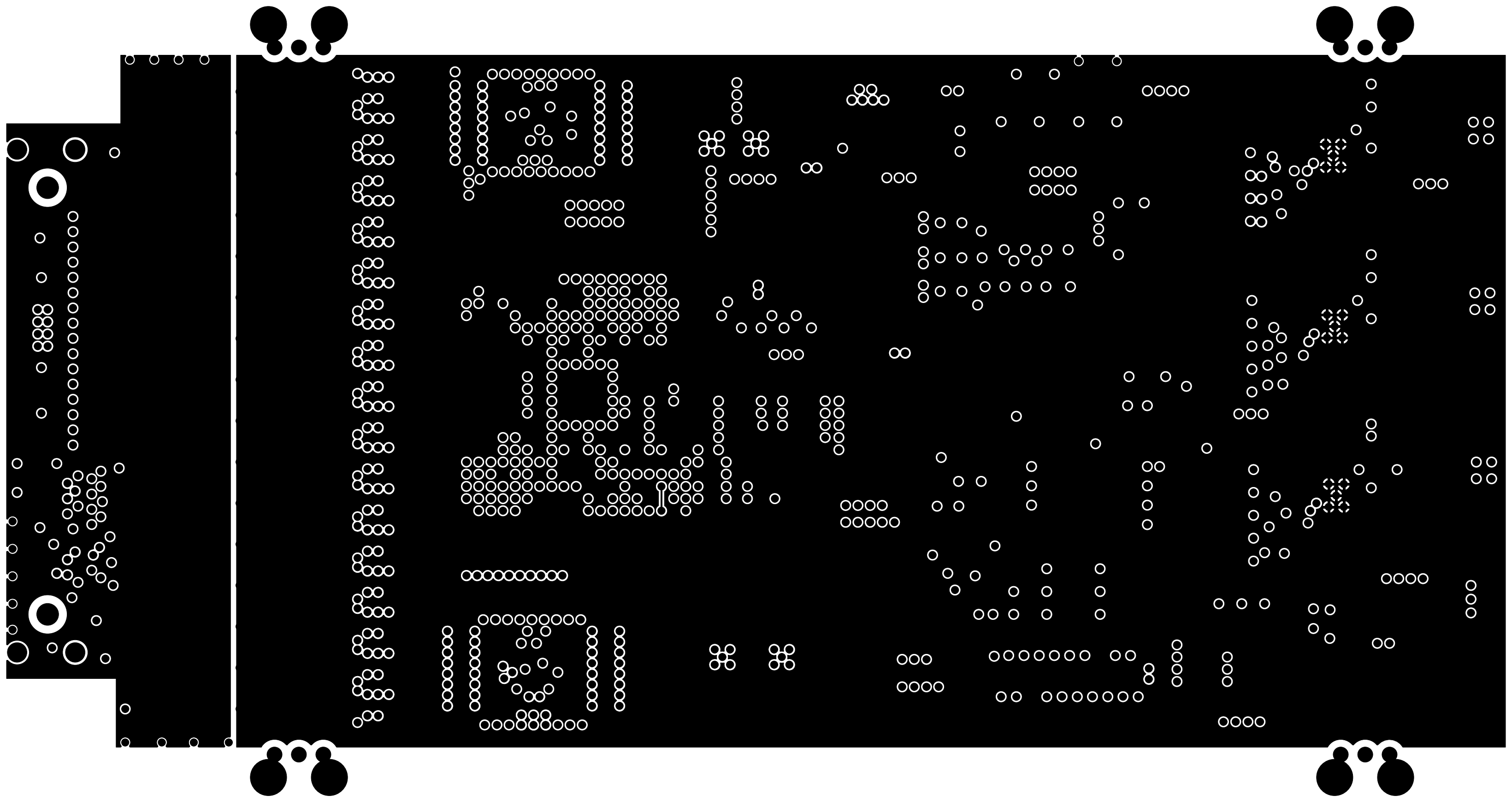
Layer Nickname Top



Jobname	Date	Designer	Layouter
DIRICH2	01.2017	M.Traxler	H.Kayan

Layer Nickname

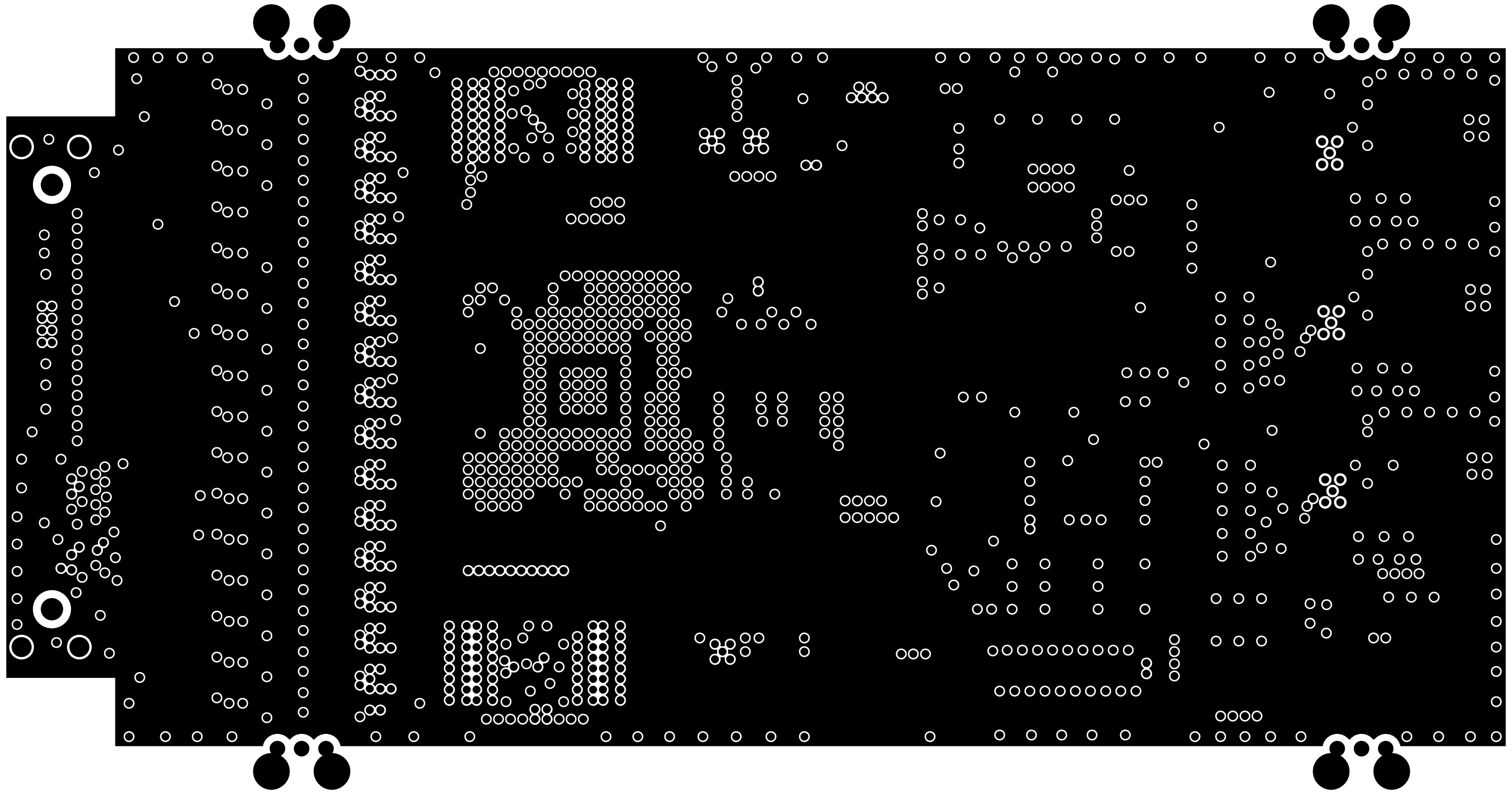
I01



Jobname	Date	Designer	Layouter
DIRICH2	01.2017	M.Traxler	H.Kayan

Layer Nickname

I02



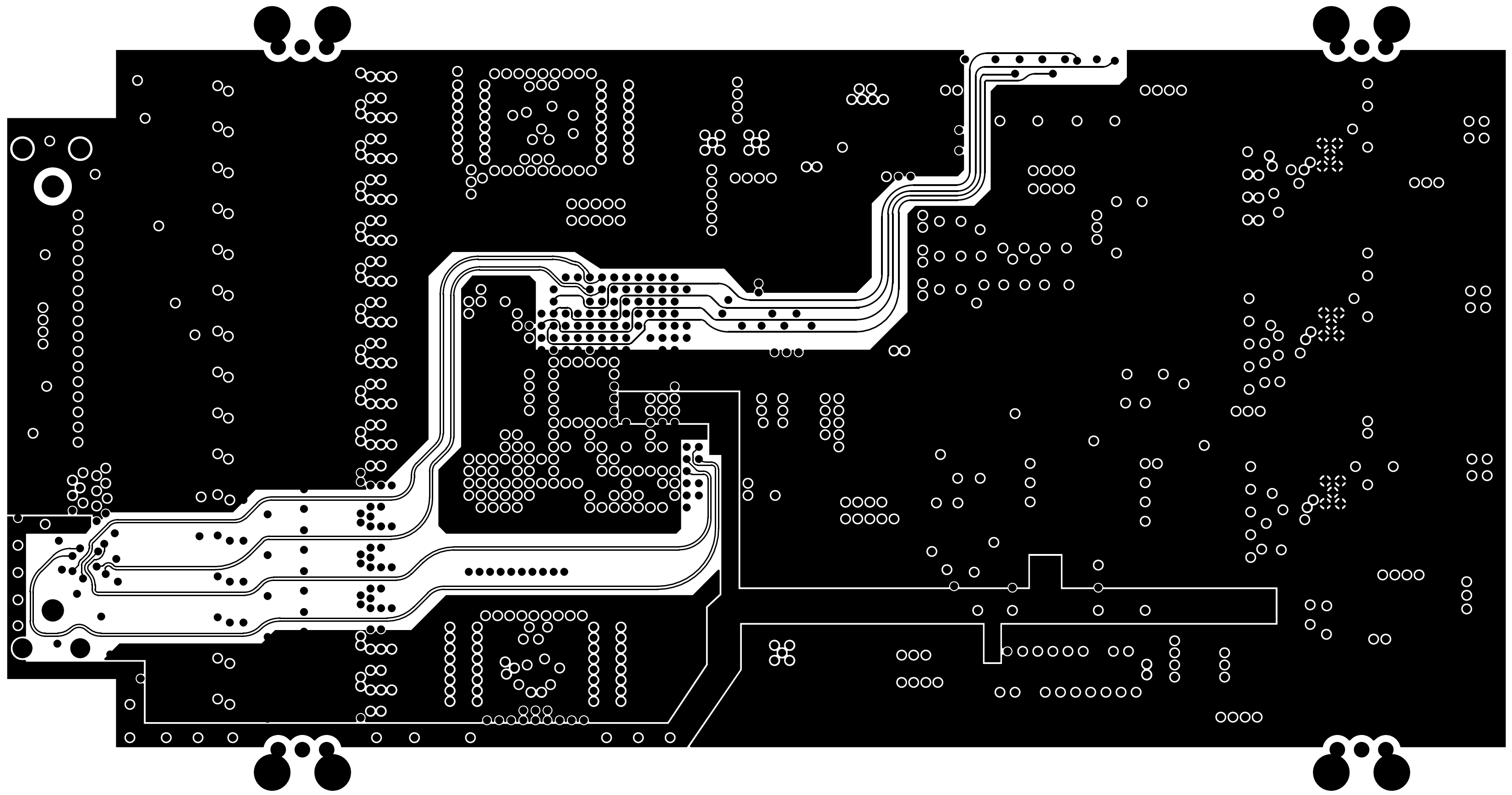
Jobname DIRICH2

Date 01.2017

Designer M.Traxler

Layouter H.Kayan

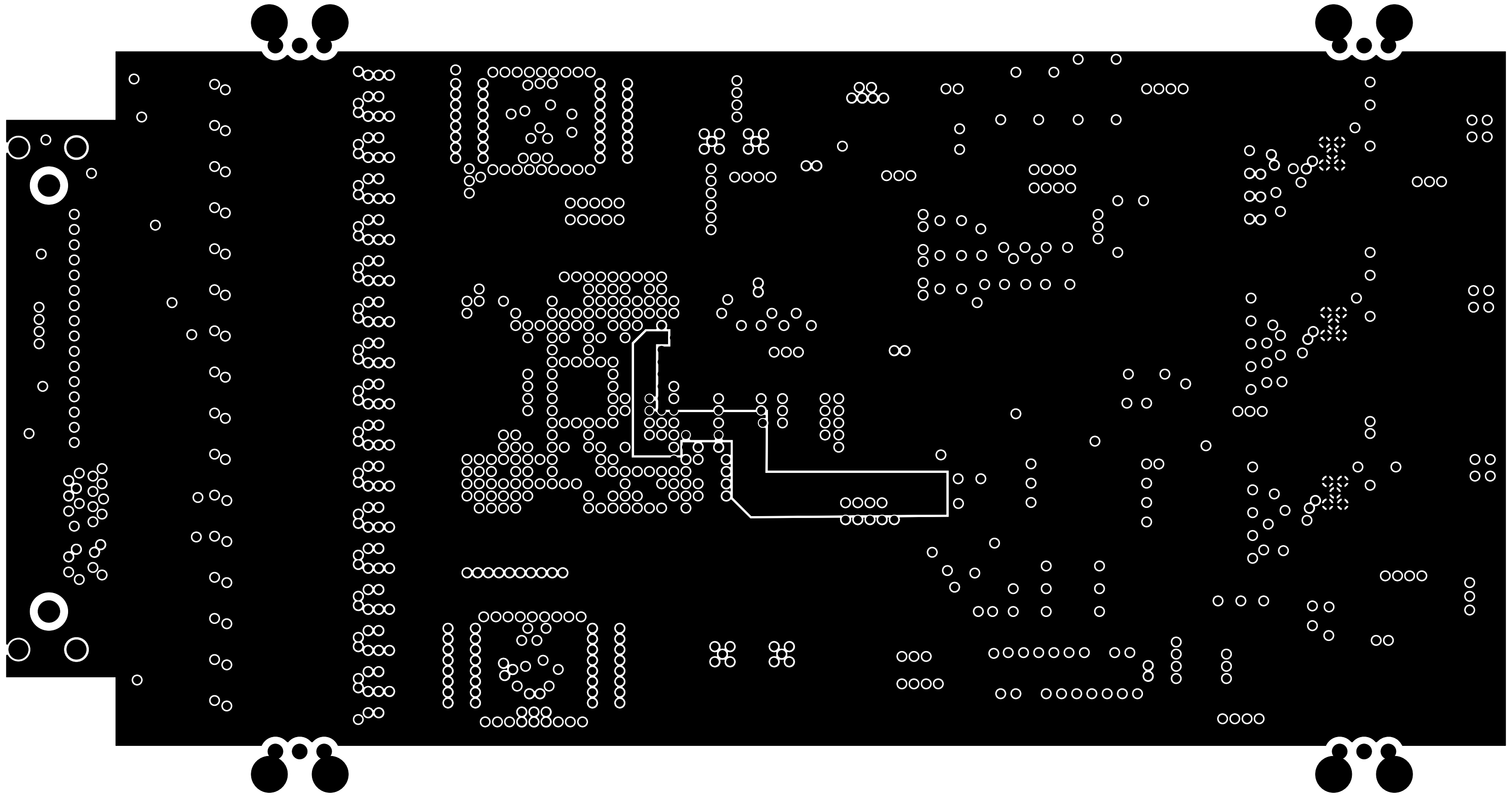
Layer Nickname I03



Jobname	Date	Designer	Layouter
DIRICH2	01.2017	M.Traxler	H.Kayan

Layer Nickname

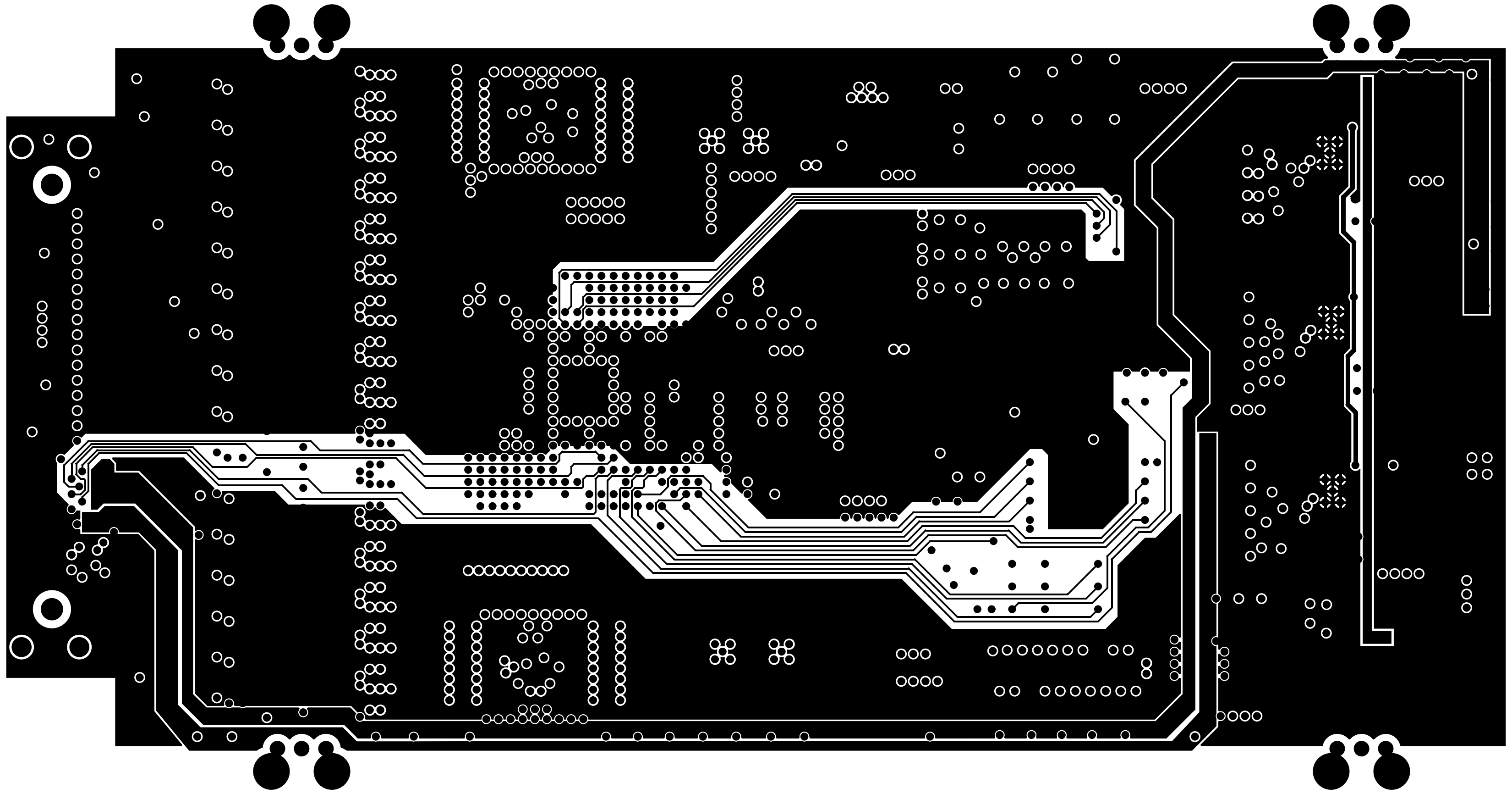
I04



Jobname	Date	Designer	Layouter
DIRICH2	01.2017	M.Traxler	H.Kayan

Layer Nickname

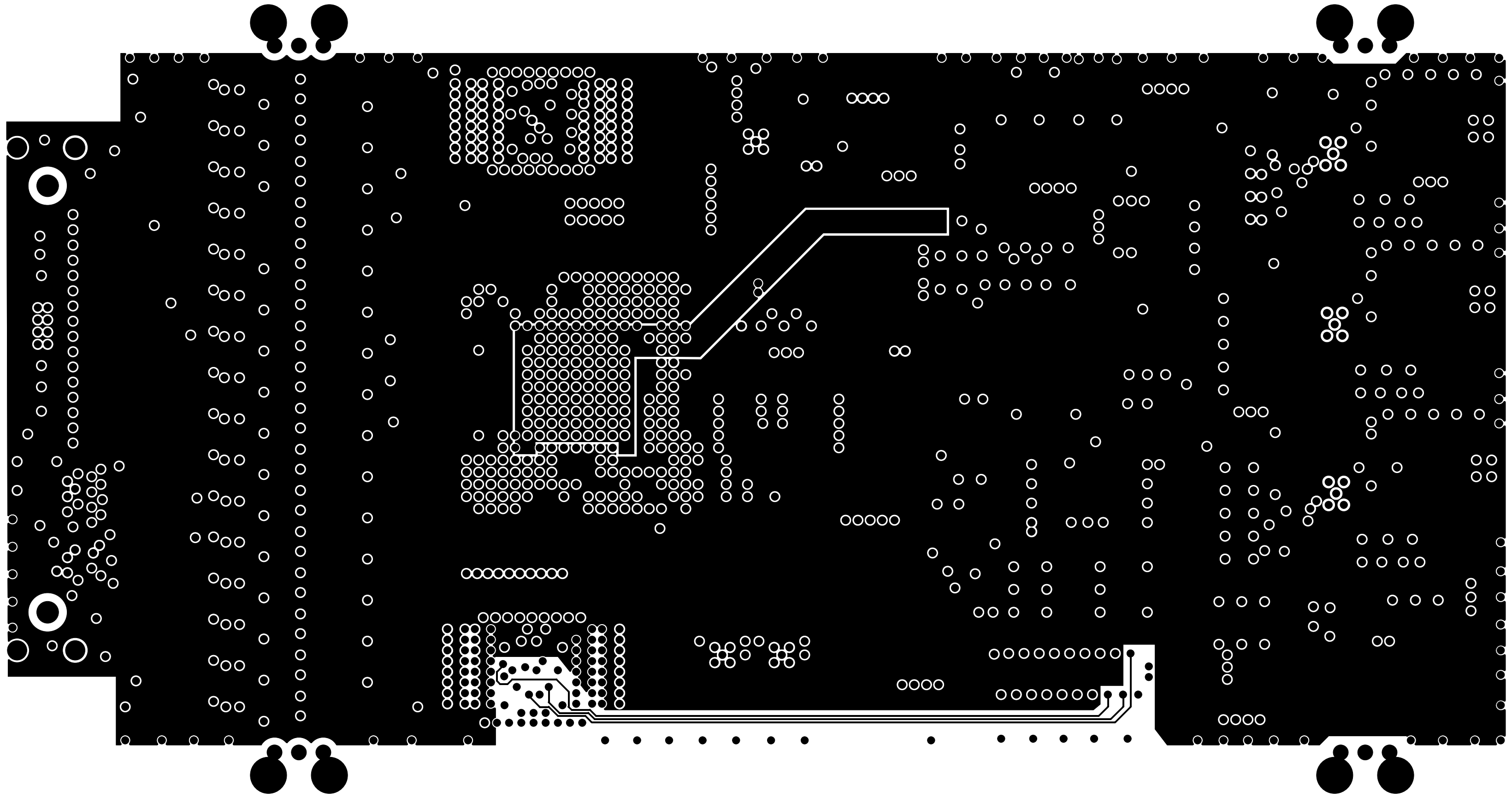
I05



Jobname	Date	Designer	Layouter
DIRICH2	01.2017	M.Traxler	H.Kayan

Layer Nickname

I06



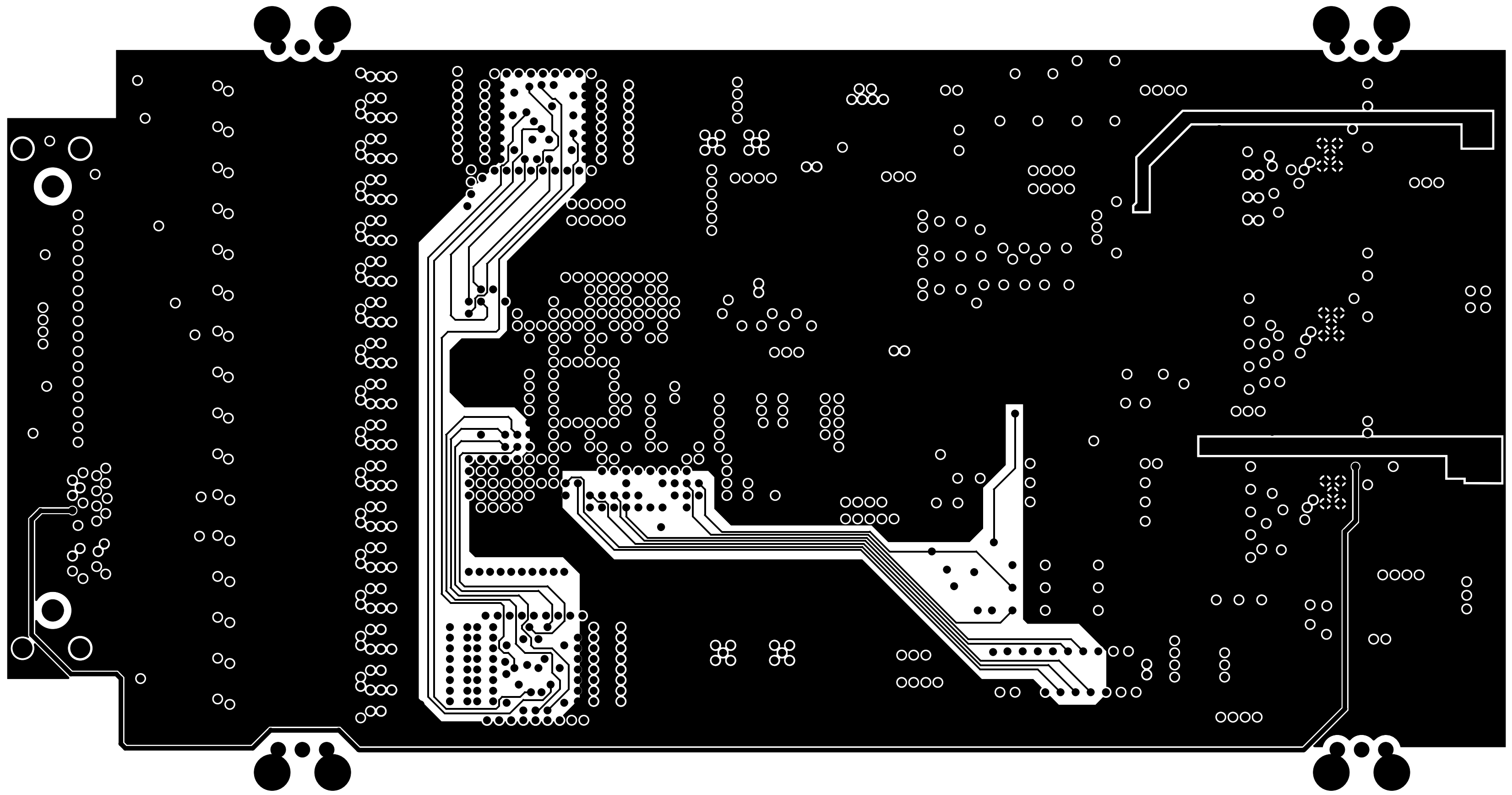
Jobname DIRICH2

Date 01.2017

Designer M.Traxler

Layouter H.Kayan

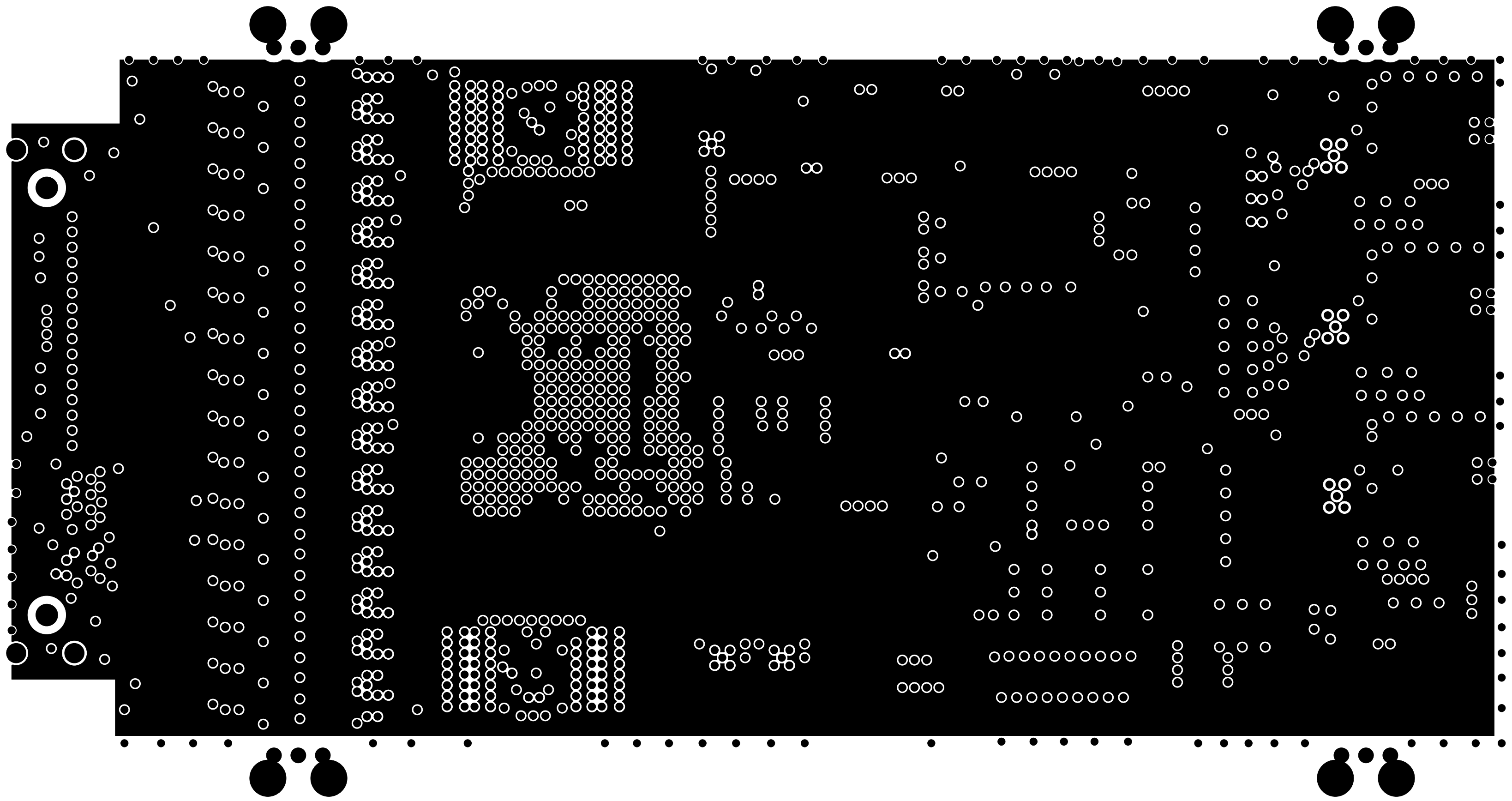
Layer Nickname I07



Jobname	Date	Designer	Layouter
DIRICH2	01.2017	M.Traxler	H.Kayan

Layer Nickname

I08



Jobname DIRICH2

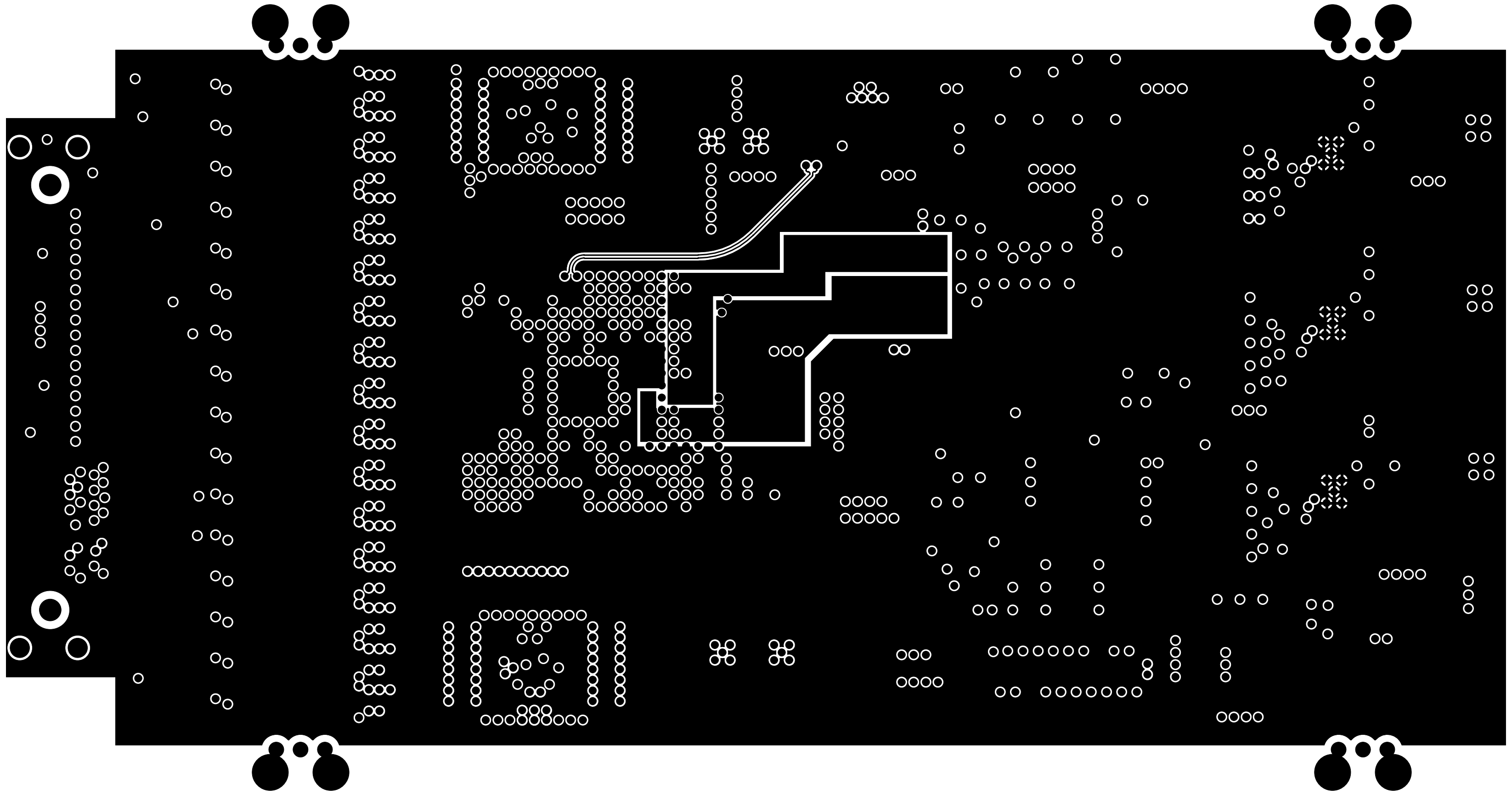
Date 01.2017

Designer M.Traxler

Layouter H.Kayan

Layer Nickname

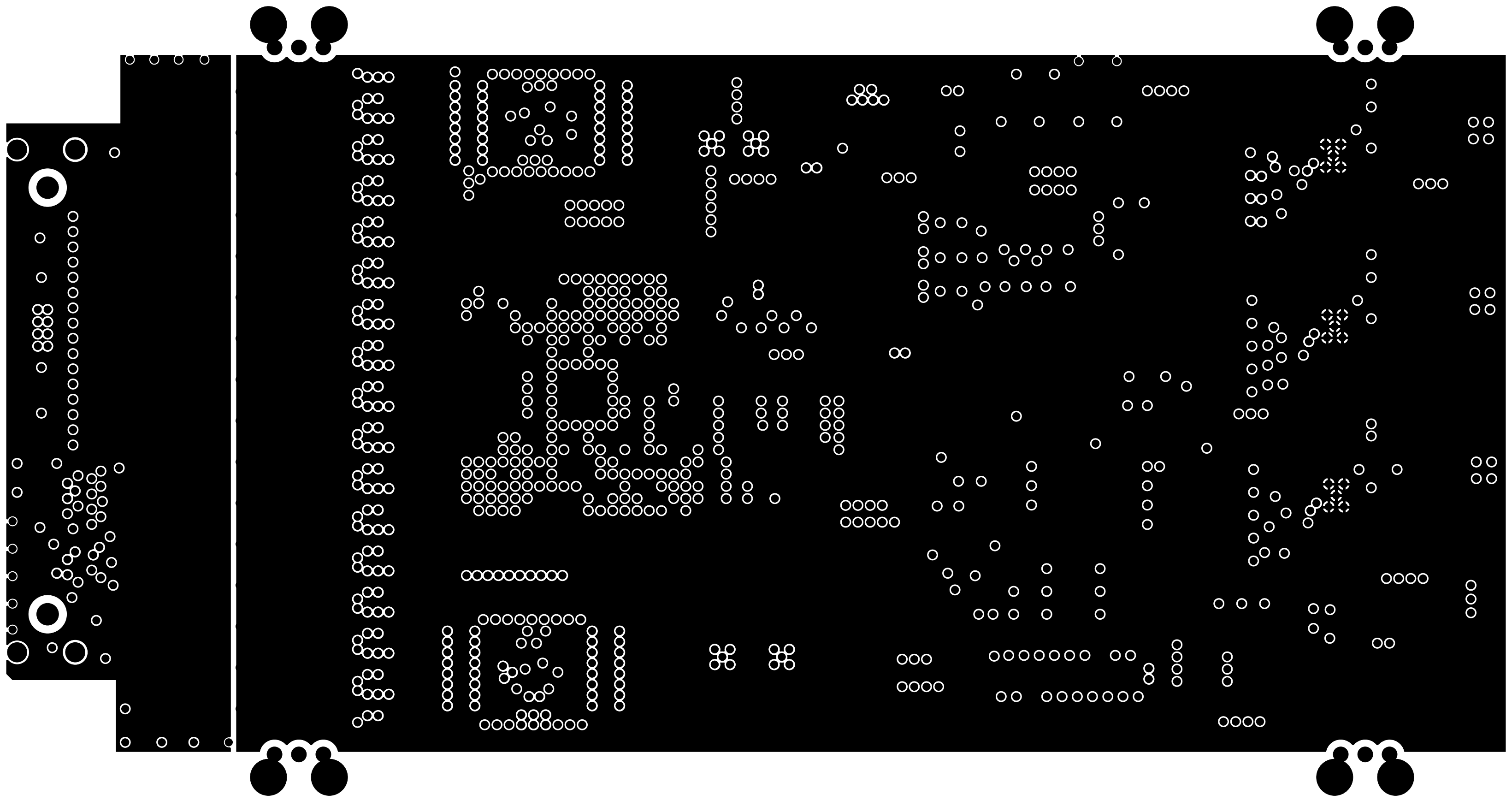
I09



Jobname	Date	Designer	Layouter
DIRICH2	01.2017	M.Traxler	H.Kayan

Layer Nickname

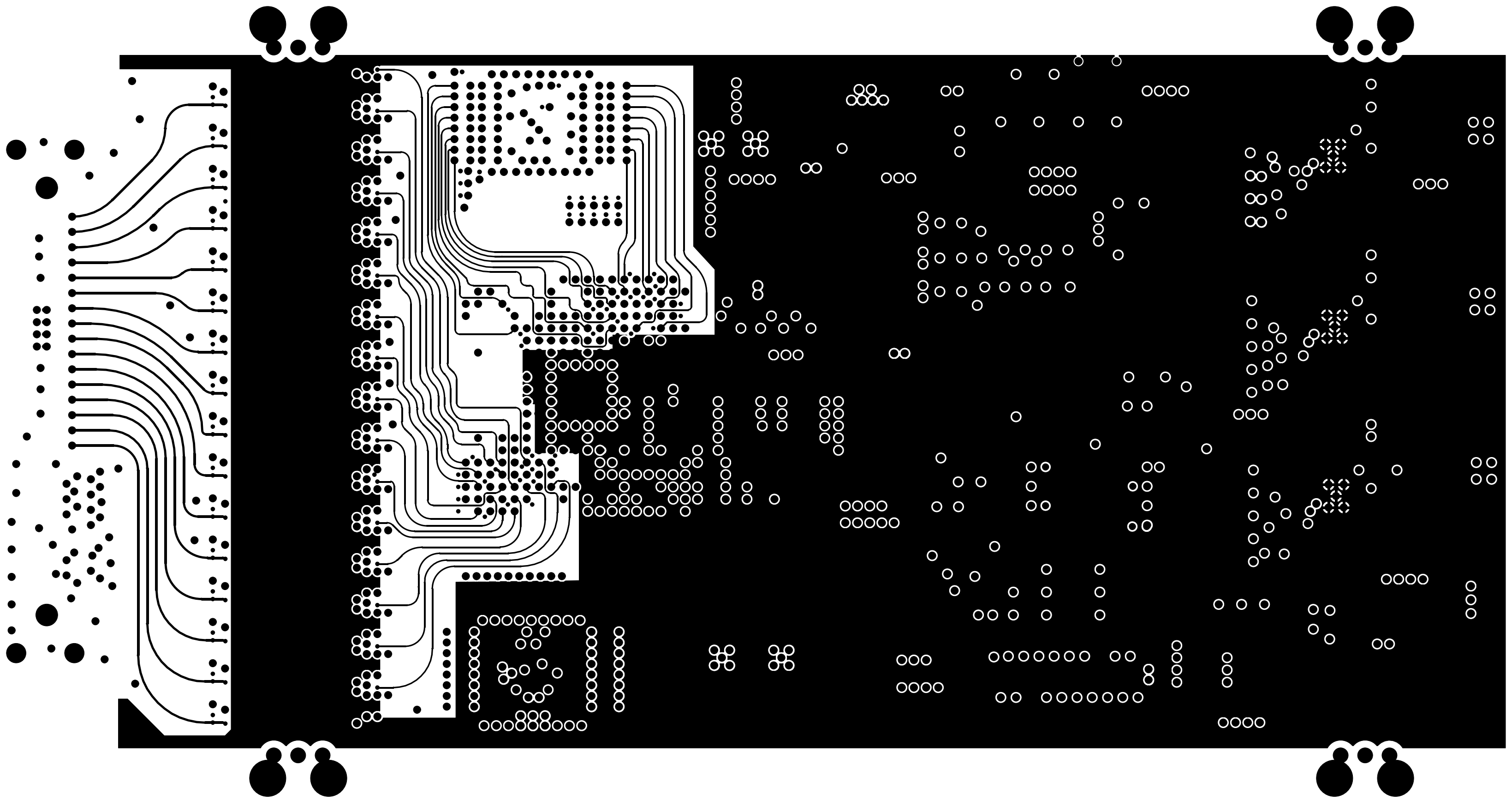
I10



Jobname	Date	Designer	Layouter
DIRICH2	01.2017	M.Traxler	H.Kayan

Layer Nickname

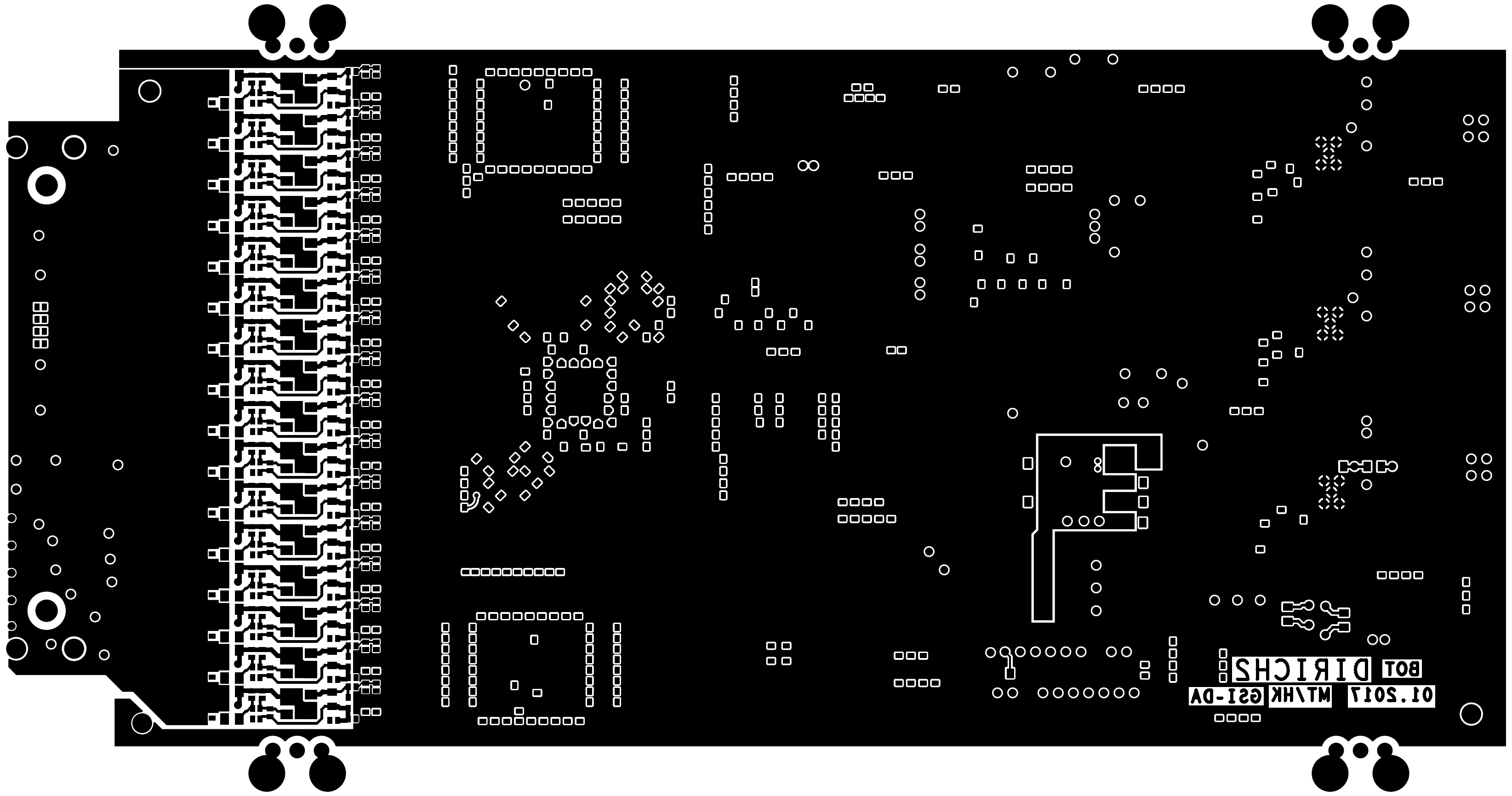
I11



Jobname	Date	Designer	Layouter
DIRICH2	01.2017	M.Traxler	H.Kayan

Layer Nickname

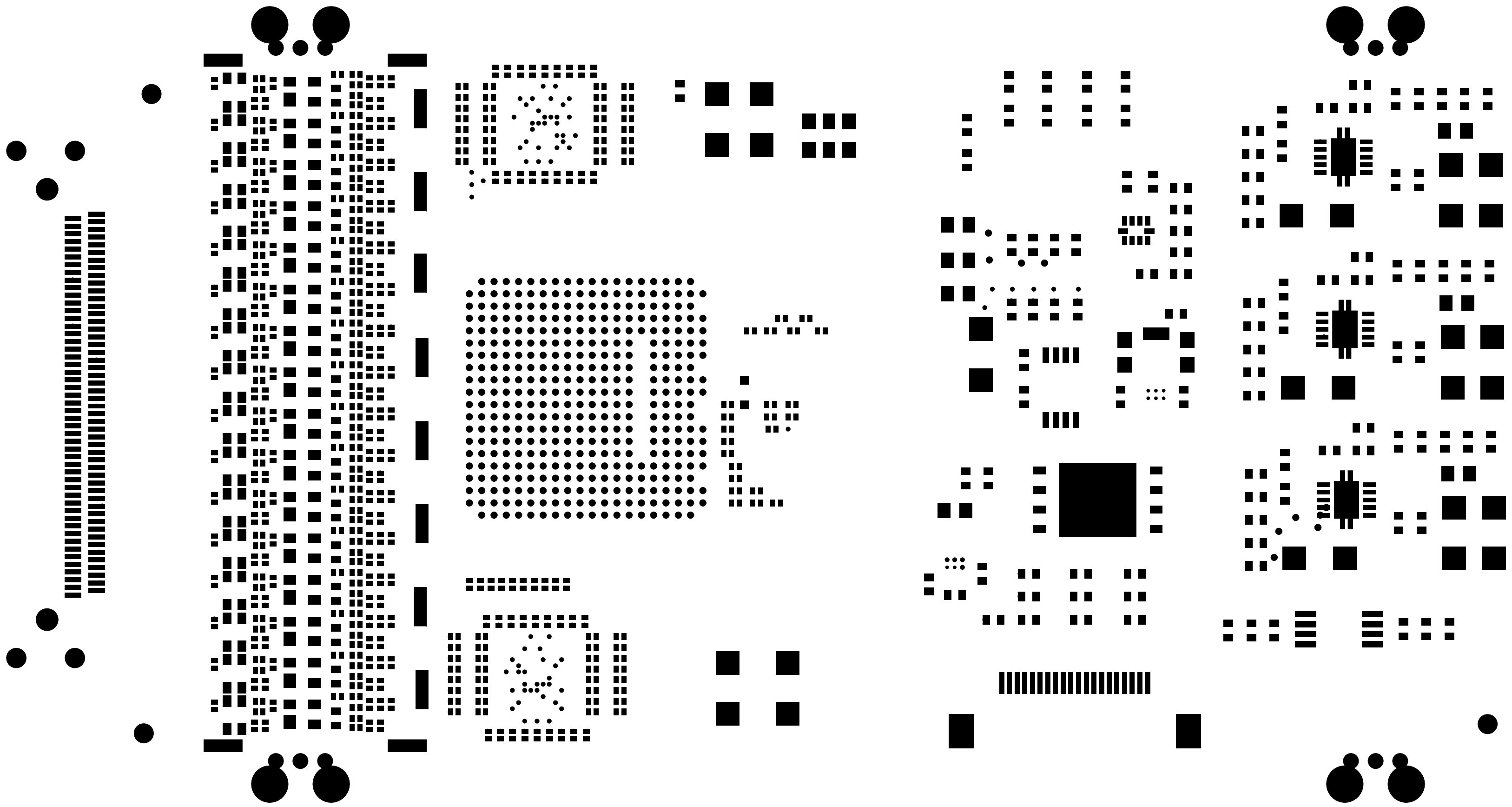
I12



Jobname	Date	Designer	Layouter
DIRICH2	01.2017	M.Traxler	H.Kayan

Layer Nickname

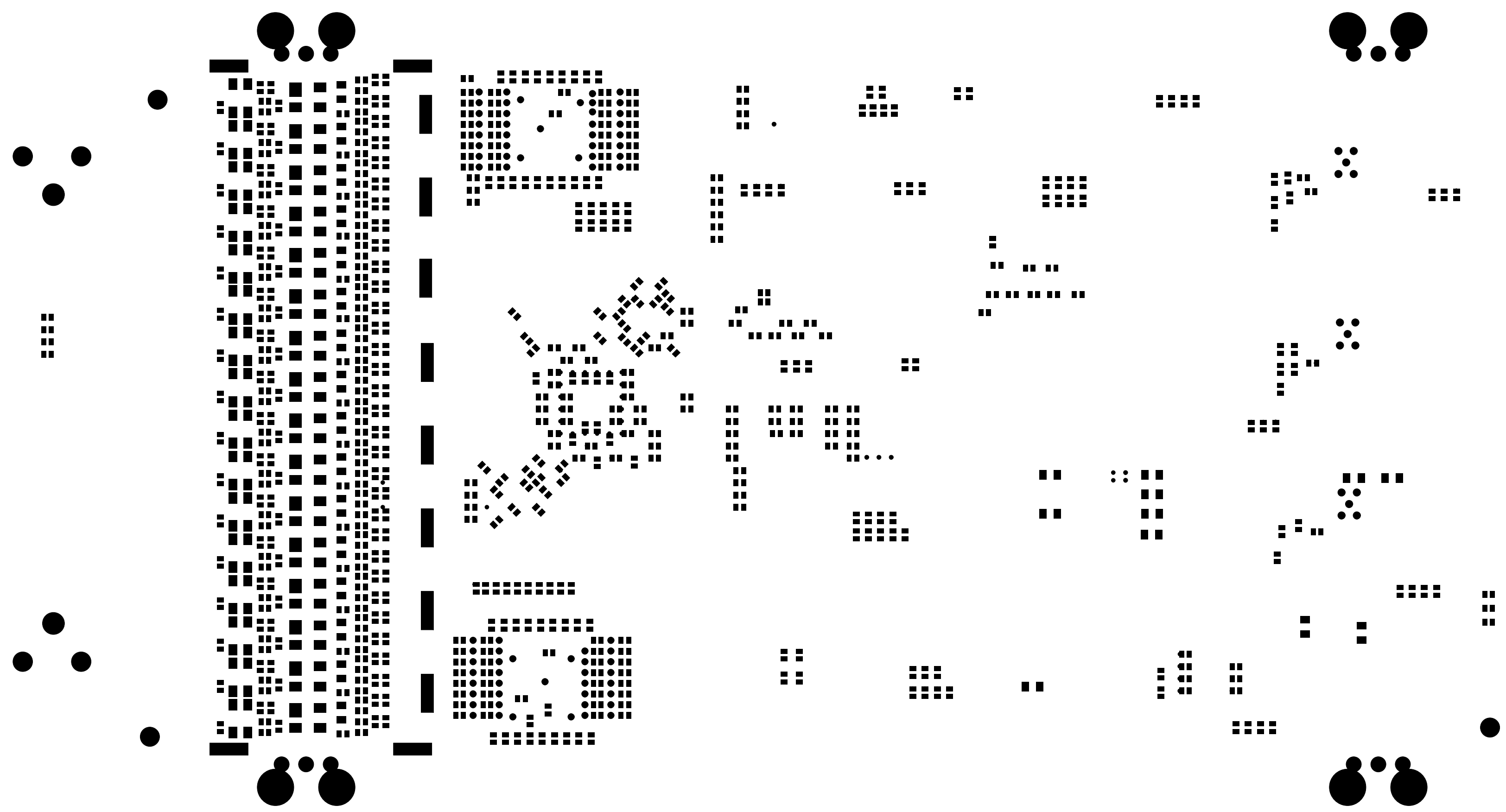
Bot



Jobname	Date	Designer	Layouter
DIRICH2	01.2017	M.Traxler	H.Kayan

Layer Nickname

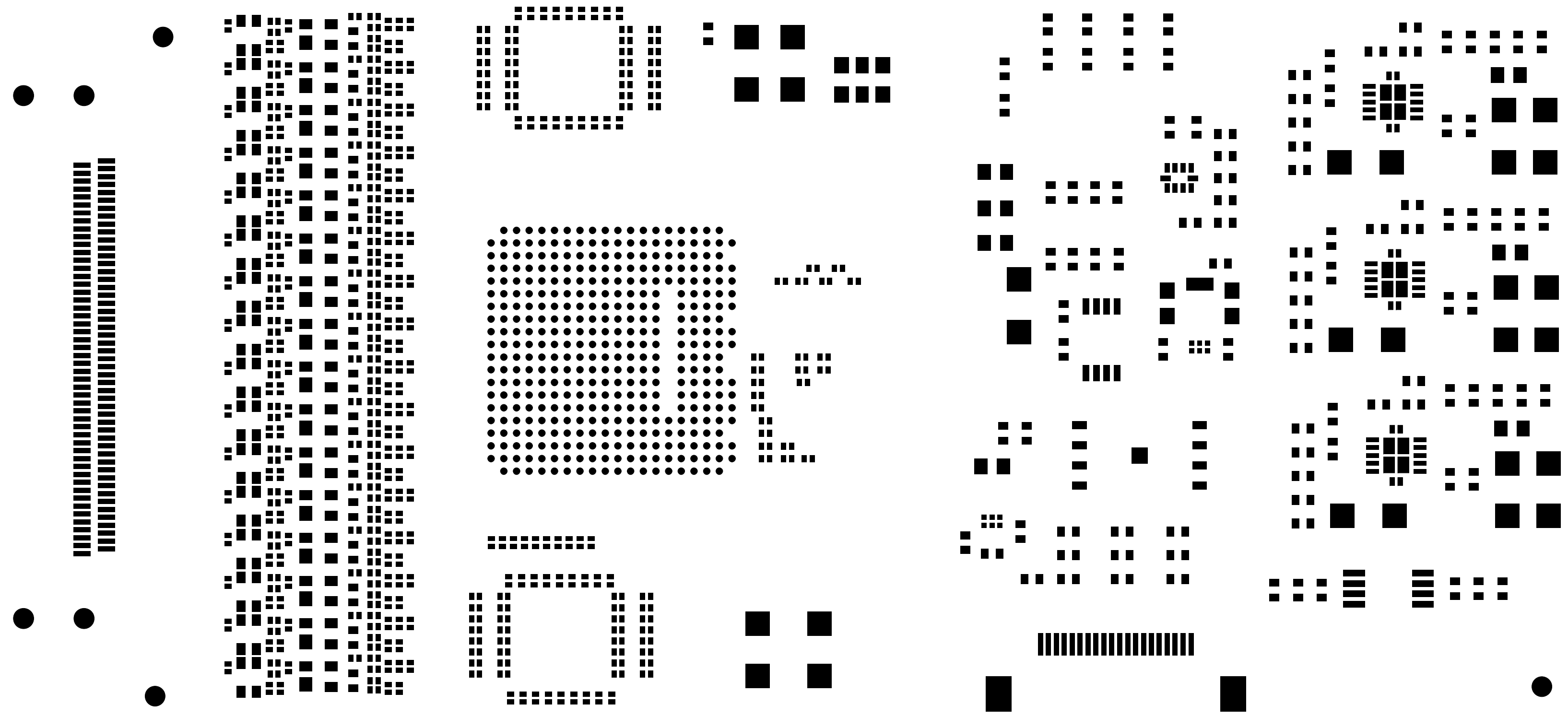
Smt



Jobname	Date	Designer	Layouter
DIRICH2	01.2017	M.Traxler	H.Kayan

Layer Nickname

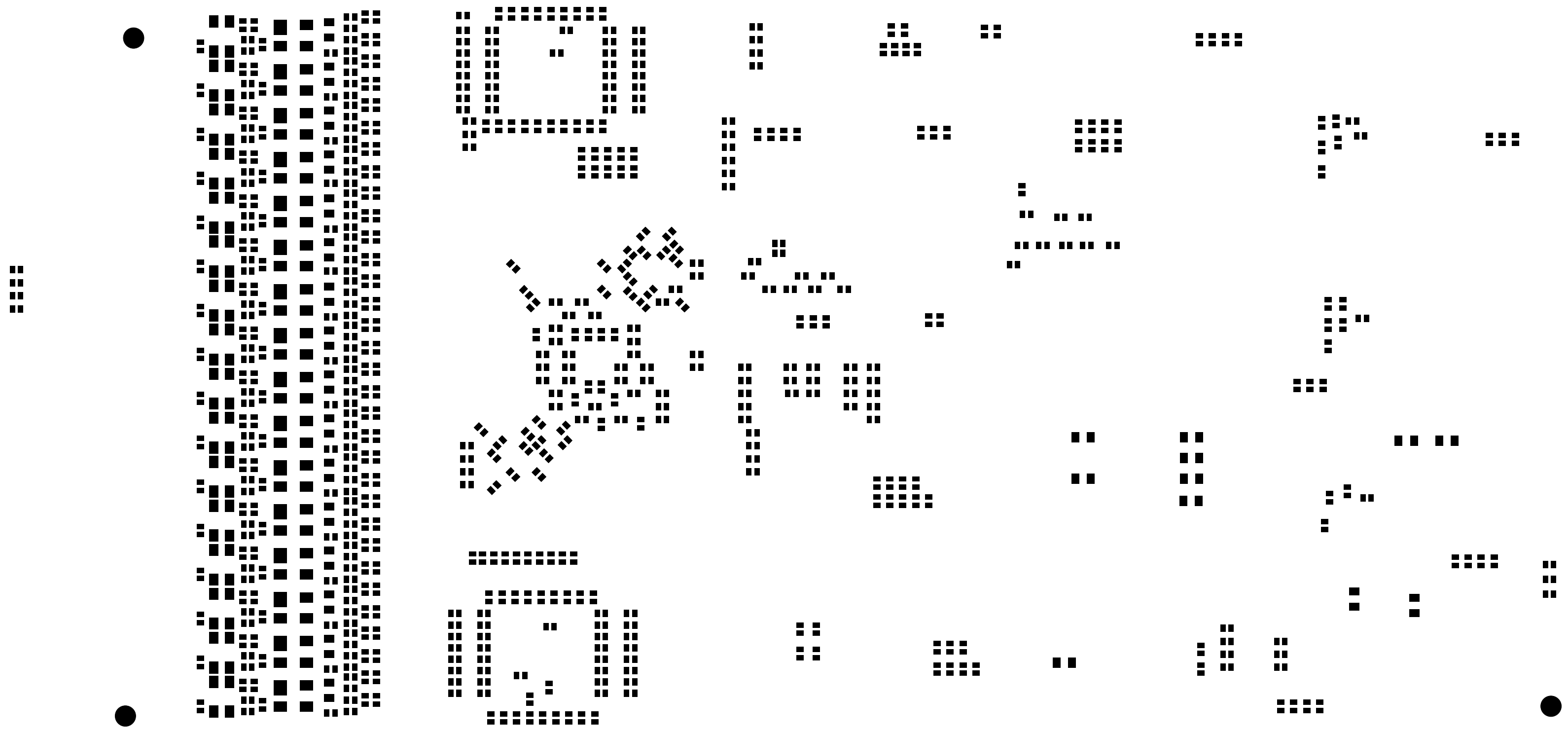
Smb



Jobname	Date	Designer	Layouter
DIRICH2	01.2017	M.Traxler	H.Kayan

Layer Nickname

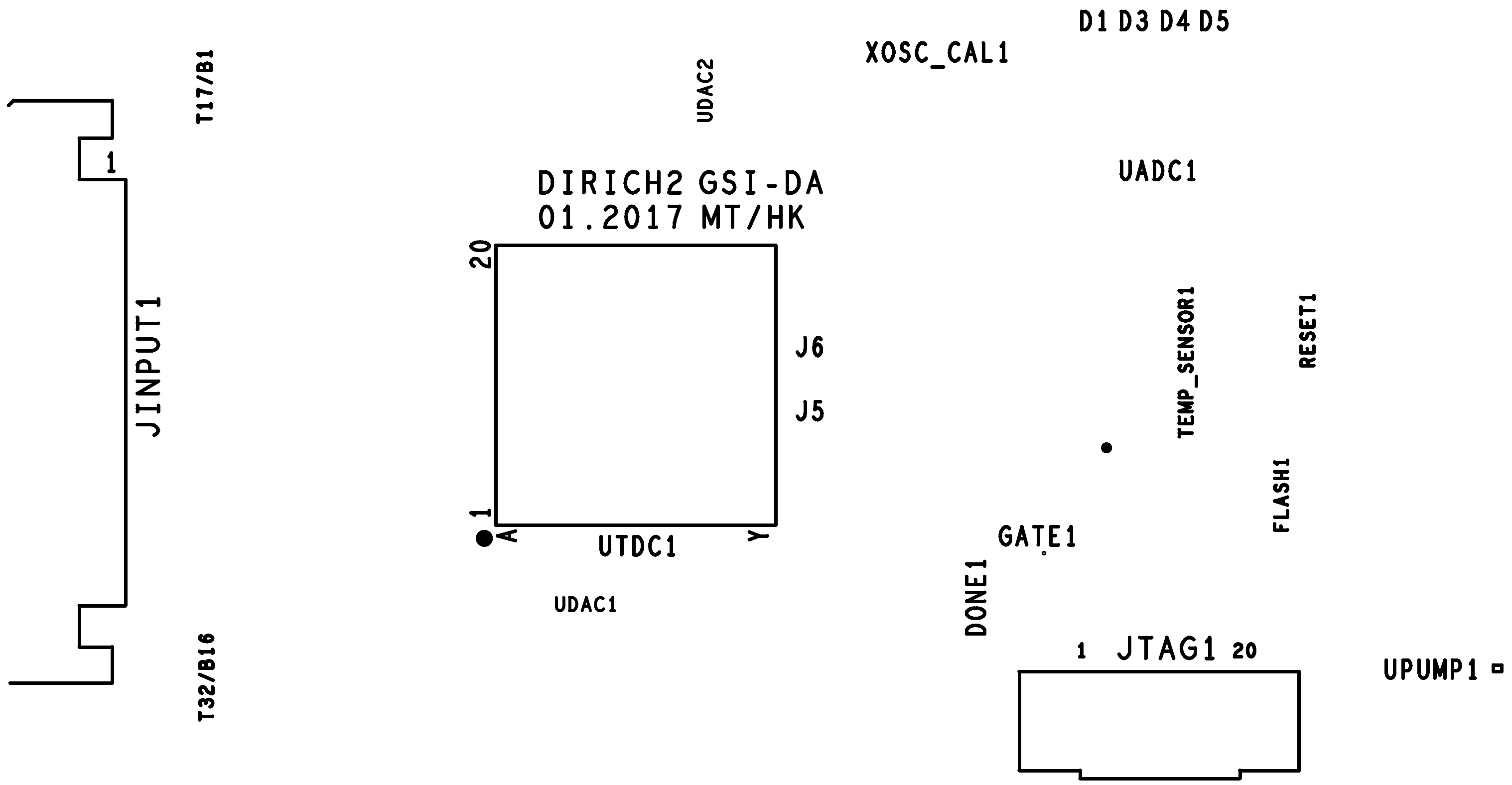
Spt



Jobname	Date	Designer	Layouter
DIRICH2	01.2017	M.Traxler	H.Kayan

Layer Nickname

Spb



Jobname	Date	Designer	Layouter
DIRICH2	01.2017	M.Traxler	H.Kayan

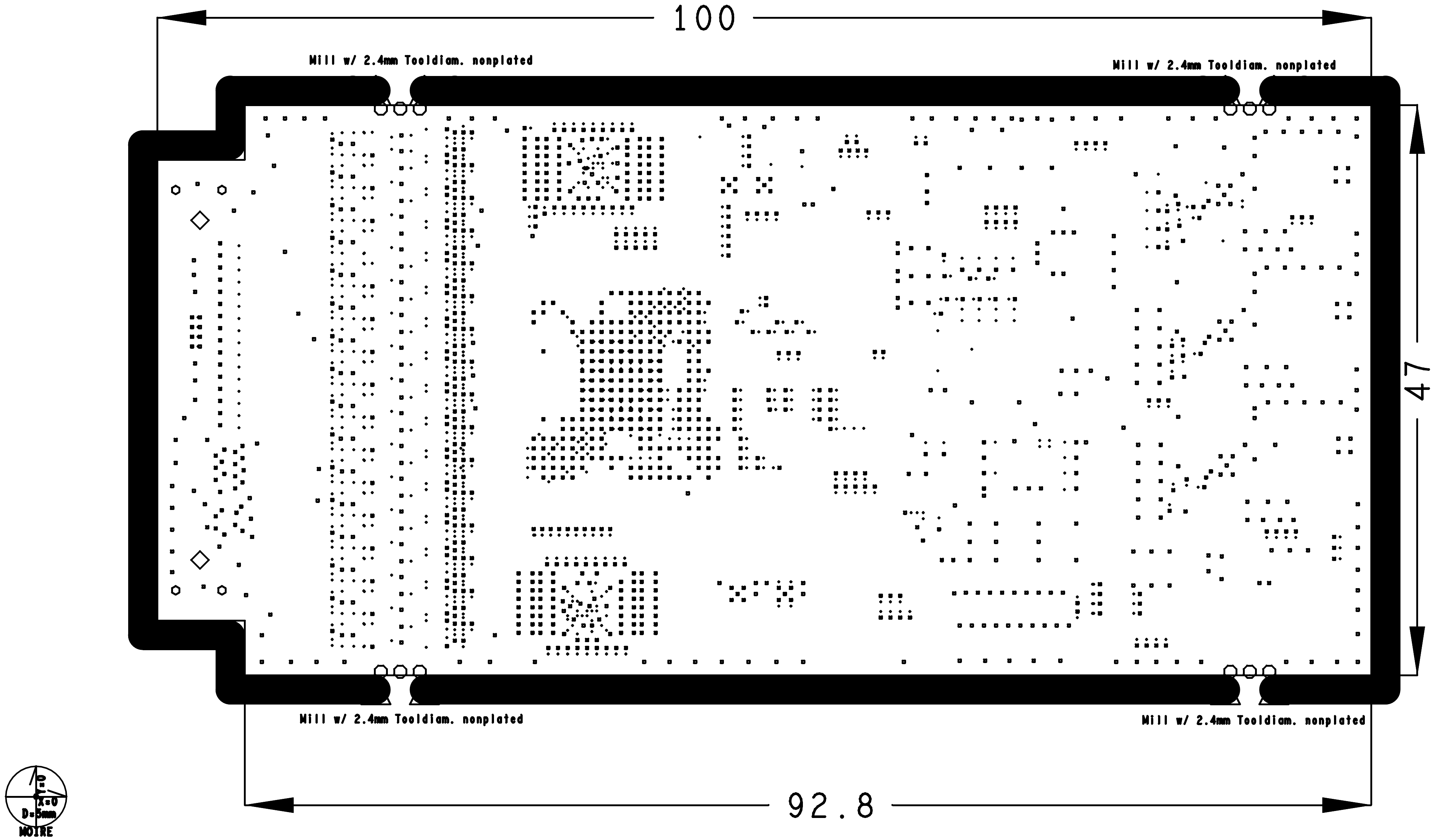
Layer Nickname

Sst

Jobname	Date	Designer	Layouter
DIRICH2	01.2017	M.Traxler	H.Kayan

Layer Nickname

Ssb



DRILL CHART: INNER12 to BOTTOM			
ALL UNITS ARE IN MILLIMETERS			
FIGURE	SIZE	PLATED	QTY
•	0.1	PLATED	1096

TOTAL HOLES: 1096

DRILL CHART: TOP to INNER1			
ALL UNITS ARE IN MILLIMETERS			
FIGURE	SIZE	PLATED	QTY
•	0.1	PLATED	1080

TOTAL HOLES: 1080

DRILL CHART: INNER1 to INNER12			
ALL UNITS ARE IN MILLIMETERS			
FIGURE	SIZE	PLATED	QTY
▪	0.2	PLATED	926

TOTAL HOLES: 926

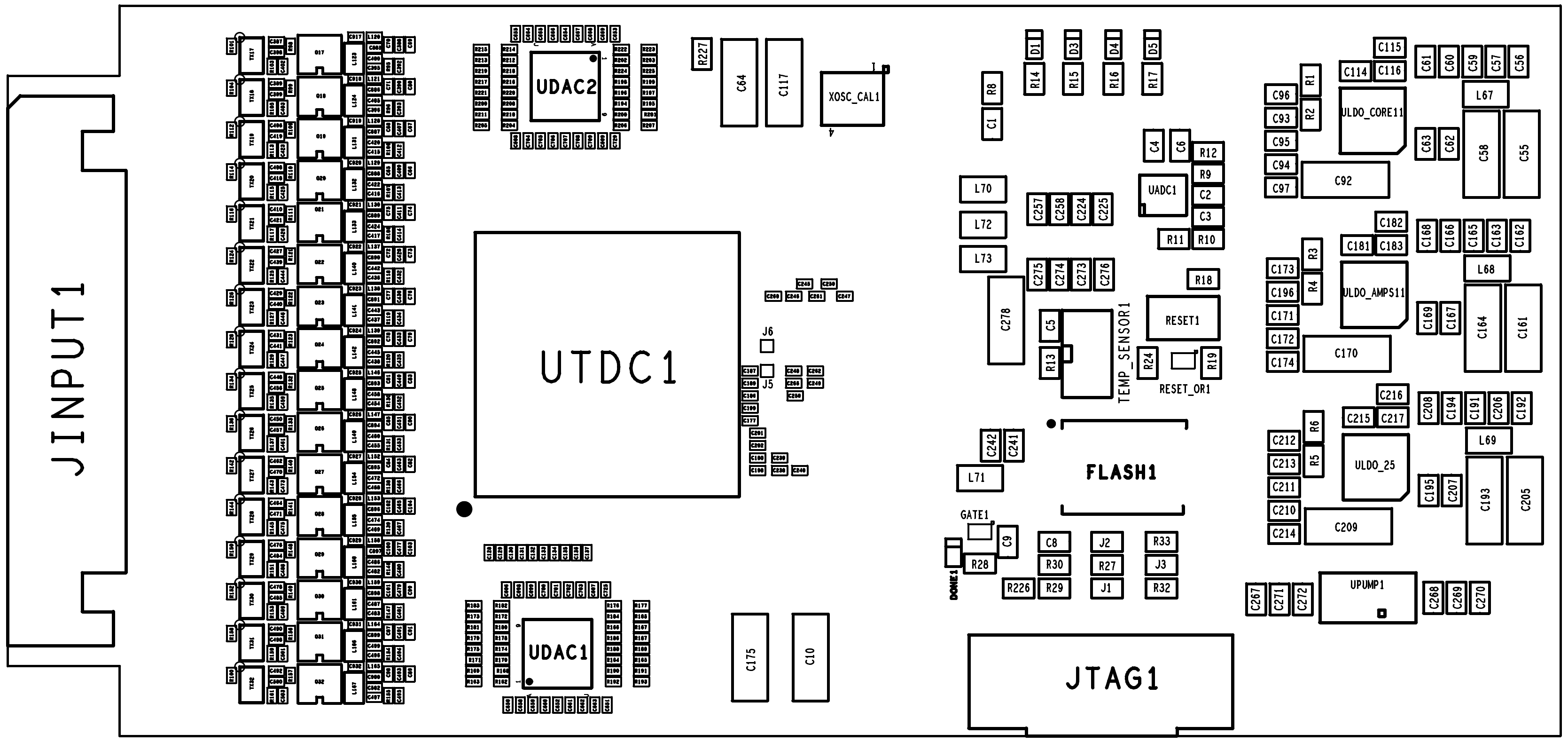
DRILL CHART: TOP to BOTTOM			
ALL UNITS ARE IN MILLIMETERS			
FIGURE	SIZE	PLATED	QTY
▪	0.2	PLATED	373
○	0.4	PLATED	1
○	0.7	PLATED	4
○	1.0	NON-PLATED	12
◇	1.45	NON-PLATED	2
△	2.4	NON-PLATED	8

TOTAL HOLES: 400

Jobname	Date	Designer	Layouter
DIRICH2	01.2017	M.Traxler	H.Kayan

Layer Nickname

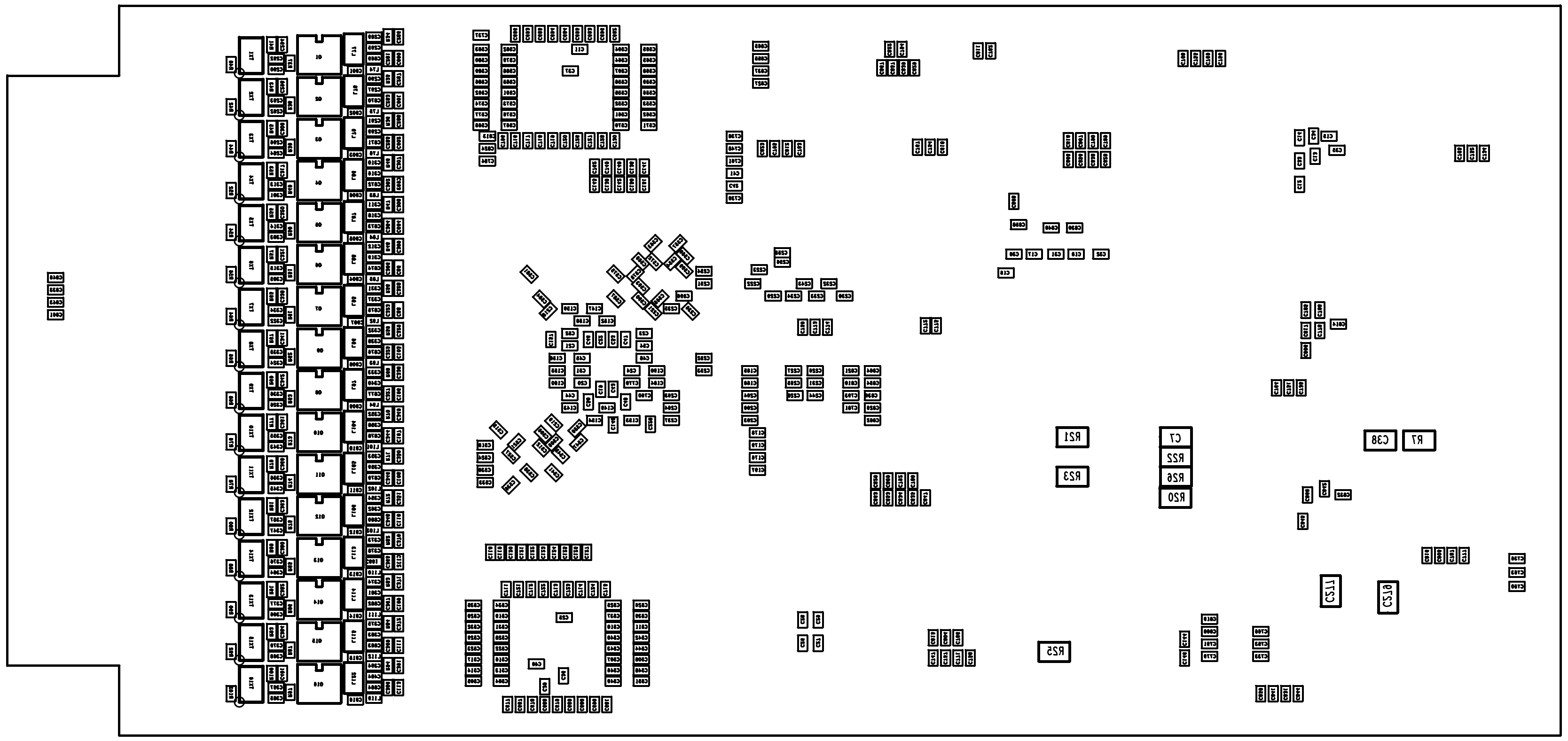
Drd



Jobname	Date	Designer	Layouter
DIRICH2	01.2017	M.Traxler	H.Kayan

Layer Nickname

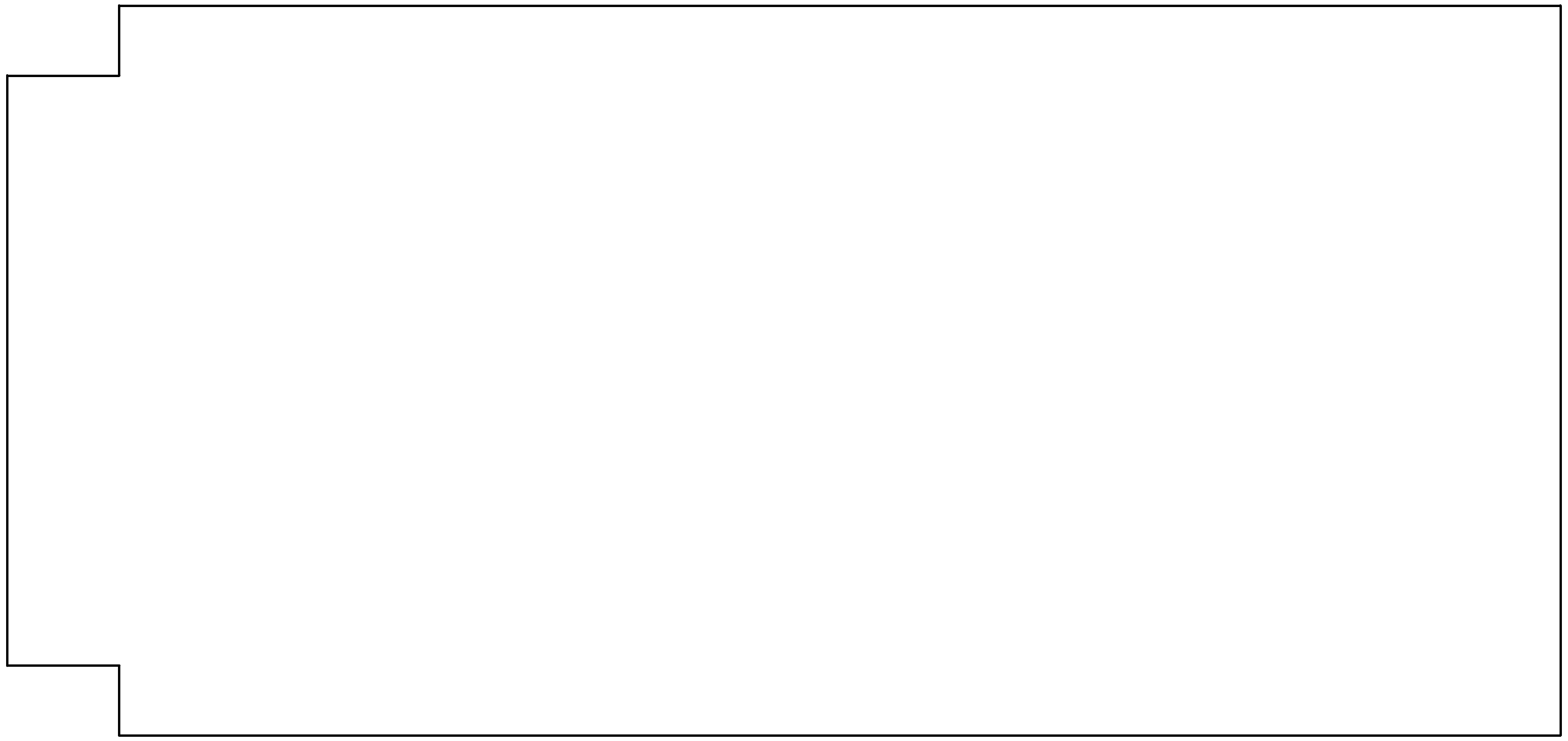
Ast



Jobname	Date	Designer	Layouter
DIRICH2	01.2017	M.Traxler	H.Kayan

Layer Nickname

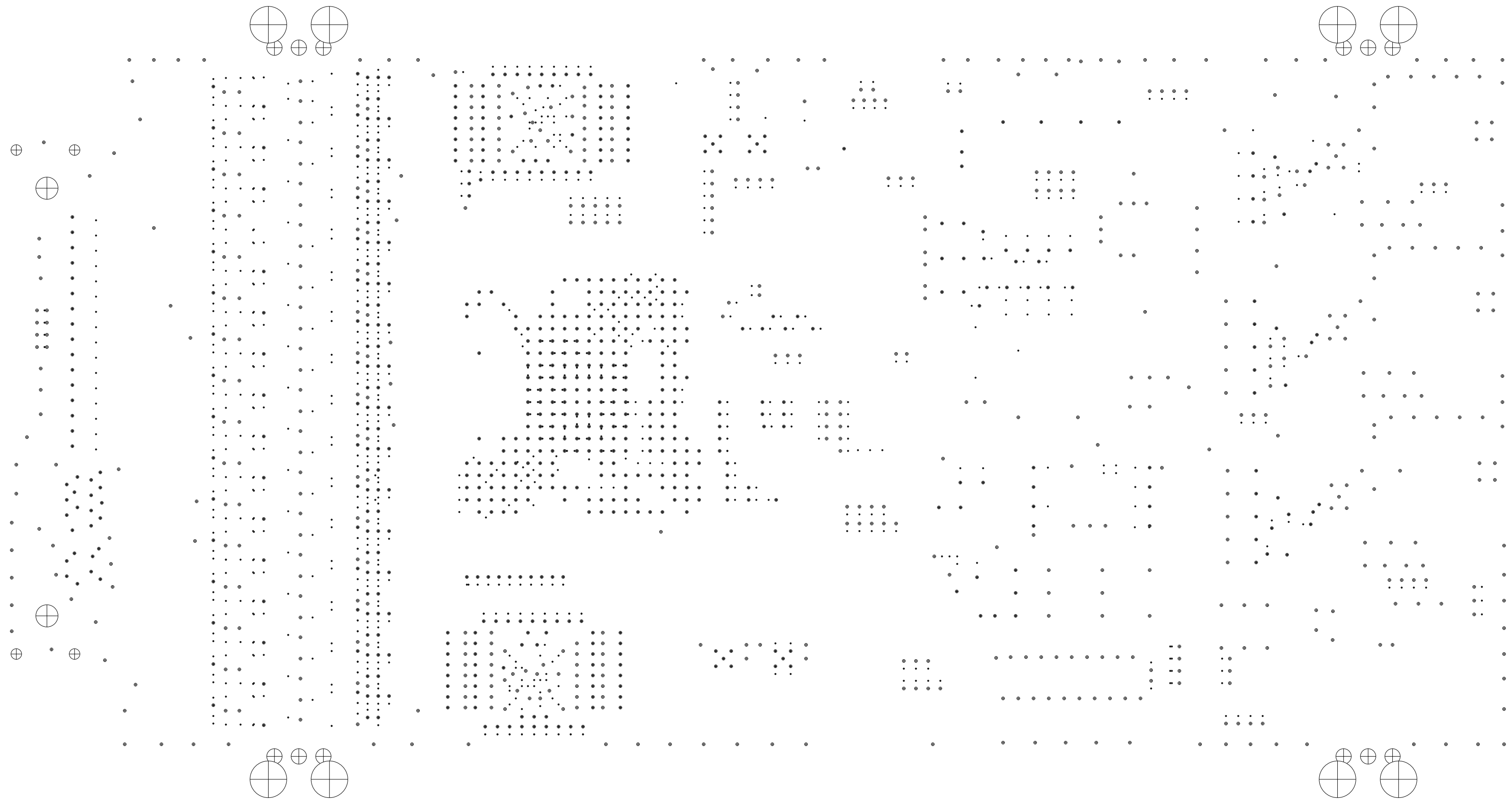
Asb

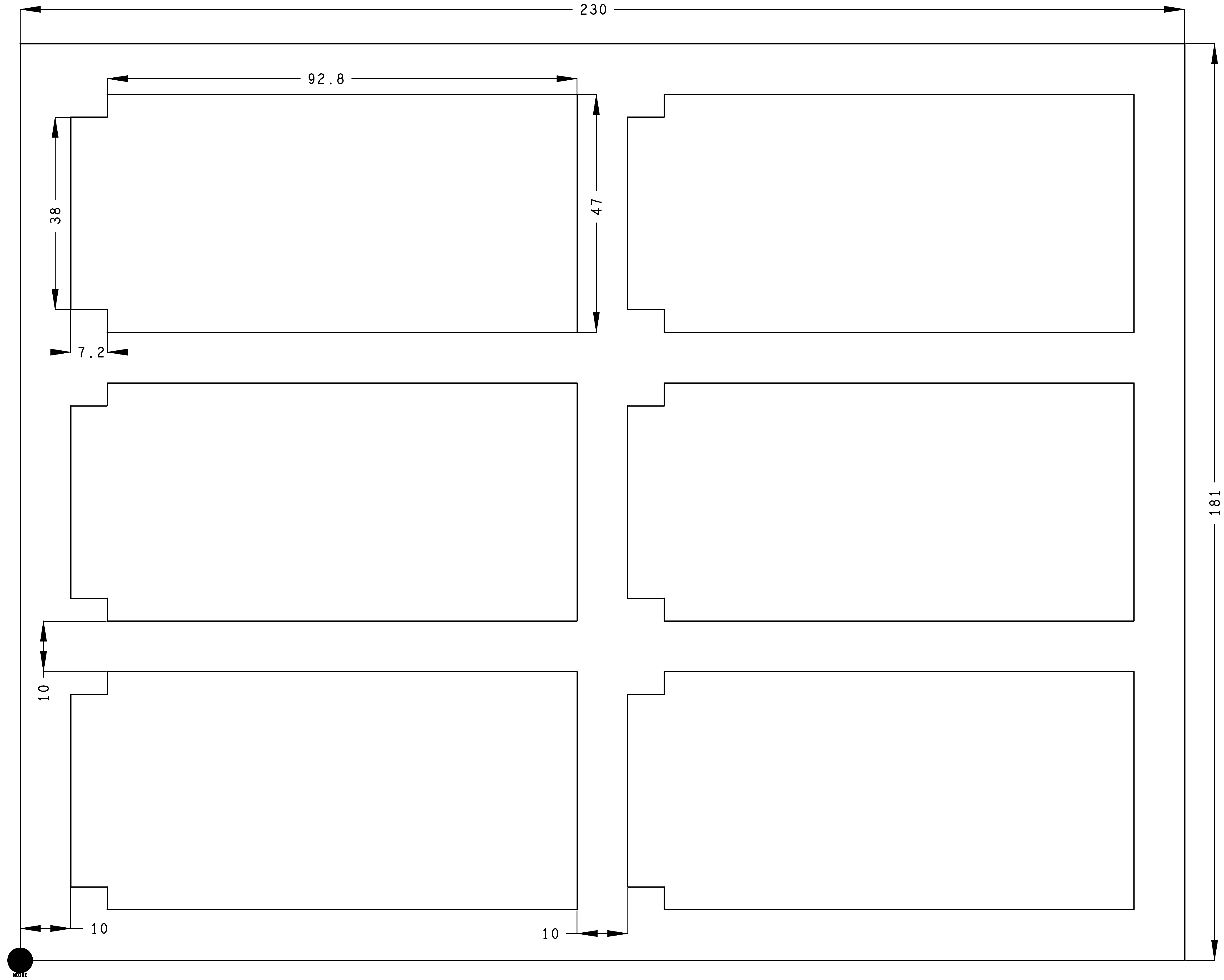


Jobname	Date	Designer	Layouter
DIRICH2	01.2017	M.Traxler	H.Kayan

Layer Nickname

Not





Jobname DIRICH2

Date 01.2017

Designer M.Traxler

Layouter H.Kayan

Layer Nickname

Fab

HDI14

Build Up HDI

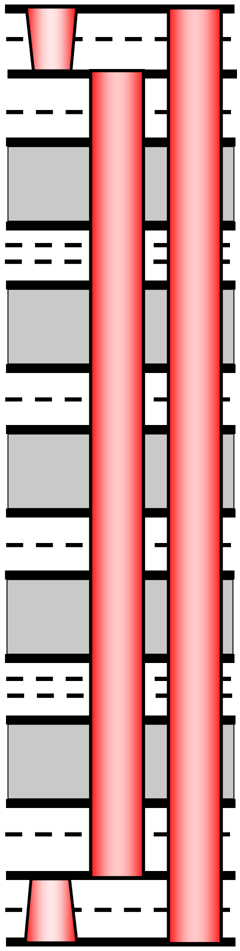
14 - Layers

WE-Articel No.: 1 + 12B + 1

Customer: GSI DIRICH1

CBT SH

Customer	WE	layer description / configuration	Raw-Material	CU	PREPREG	Dielectric constant [εr]	Final Thickness [µm]	Customer requirements [µm]
	TOP/VS	SIG/GND	Foil	12 µm	1)		12	
					1 x 1080	3.5	68	
	2	SIG/GND	Foil	12 µm			30	
					1 X 1080	3.5	70	
	3	SIG/GND		17.5 µm			16	
			0.125 mm			4.0	125	
	4	GND		17.5 µm			16	
					2 X 1080	3.7	134	
	5	SIG/GND		17.5 µm			16	
			0.100 mm			3.8	100	
	6	GND		17.5 µm			16	
					1 X 1080	3.5	65	
	7	SIG/GND		17,5 µm			16	
			0.100 mm			3.8	100	
	8	GND		17,5 µm			16	
					1 X 1080	3.8	65	
	9	SIG/GND		17.5 µm			16	
			0.100 mm			3.8	100	
	10	GND		17.5 µm			16	
					2 X 1080	3.7	134	
	11	S1		17.5 µm			16	
			0.125 mm			4.0	125	
	12	GND		17.5 µm			16	
					1 X 1080	3.5	70	
	13	SIG/GND	Foil	12 µm			30	
					1 x 1080	3.5	68	
	BOT/RS	SIG/GND	Foil	12 µm	1)		12	



Material: lowCTE Tg.150° hf

1) copper thickness outer layers: appr. 50 µm

Impedance calculation

We	S1 Zdiff 100 Ohm @ 85 / 115 / 85 µm
GSI	S1 Zdiff 92 Ohm @ 100 / 100 / 100 µm

total material thickness: 1468

Note: Lamination thickness for Prepregs depending on layout characteristics.

final lamination thickness:	1,47	+/-	0,14	mm	Date:	Engineer:
thickness with electro plated Cu:	1,55	+/-	0,15	mm	01.02.2016	Muniyappa
total thickness with soldermask	1,61	+/-	0,16	mm		
customer requirement	1,60	+/-		mm	point:	

prepared: on	by	checked: on	by	approved: on	by	revision	page:
		02.02.2016	P. Reeb			00	