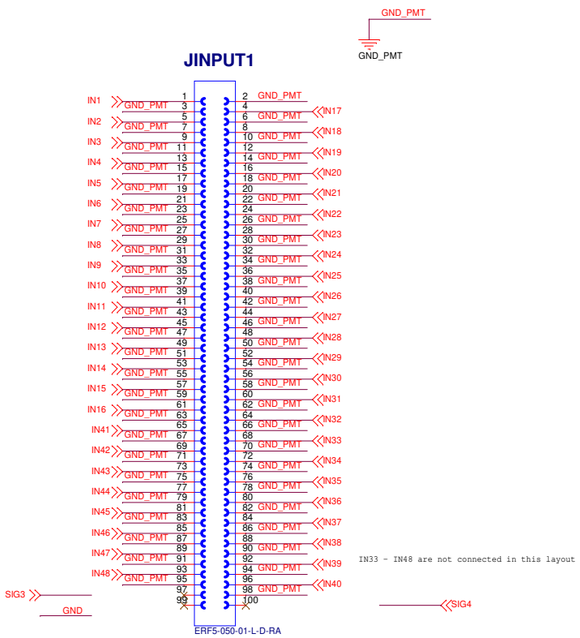
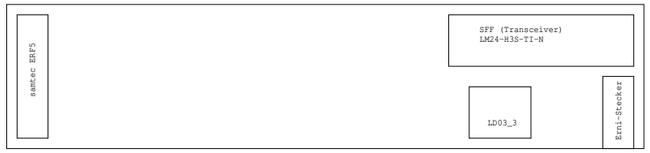
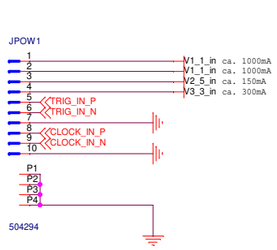
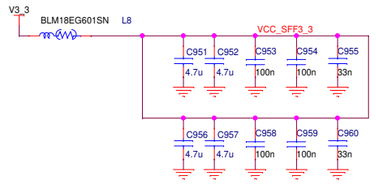


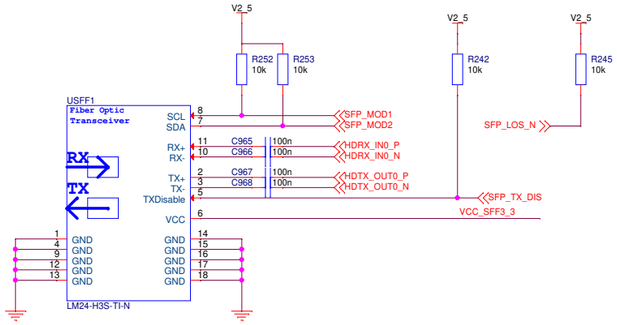
IN33 - IN48 are not connected in this layout

IN[32..1]









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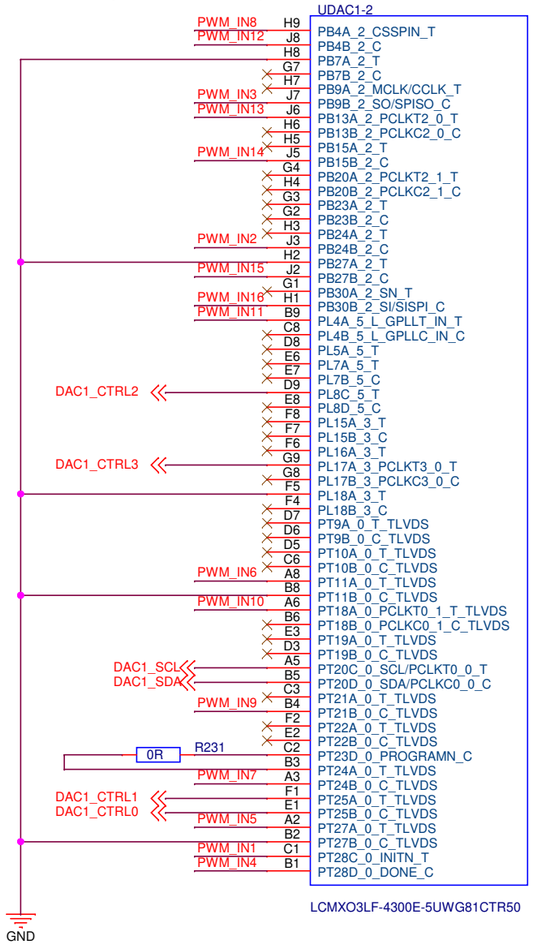
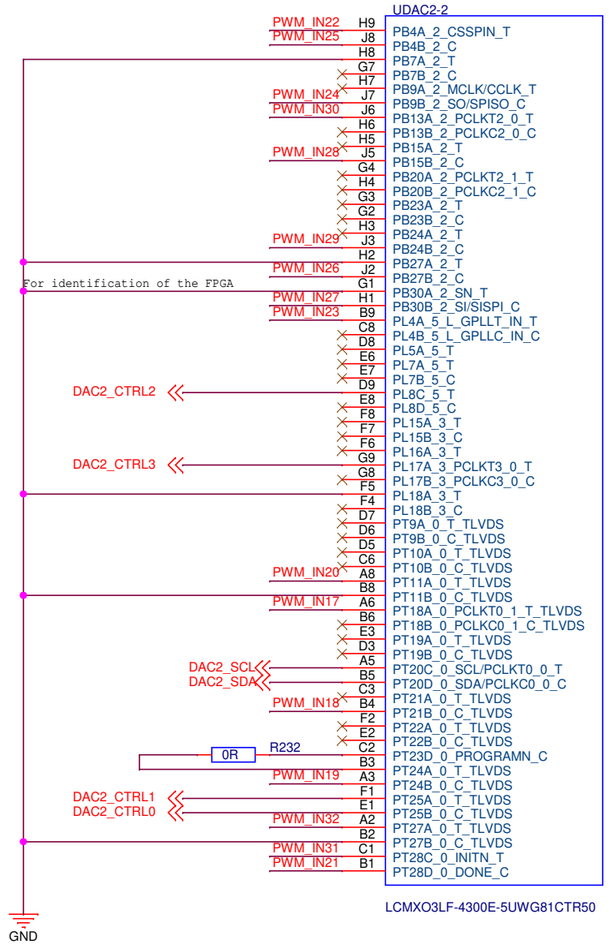
INPUT

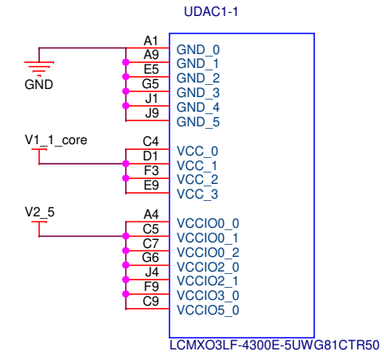
Design: K:\GSI\OB\COME_AND_KISS\DIRICH\DIRICH5S1\DIRICH5S1.DSN
Modified: Tuesday, March 23, 2021
Designer: M.Traxler
Size: A2
Page: 1 / 9
Layouter: H.Kavan

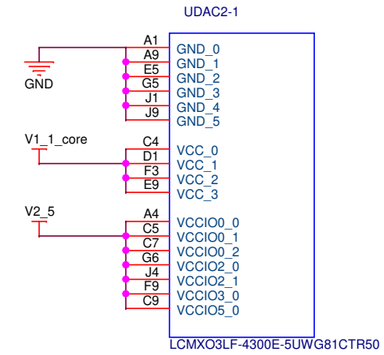
PWM_IN:
these are outputs from this FPGAs point of view....

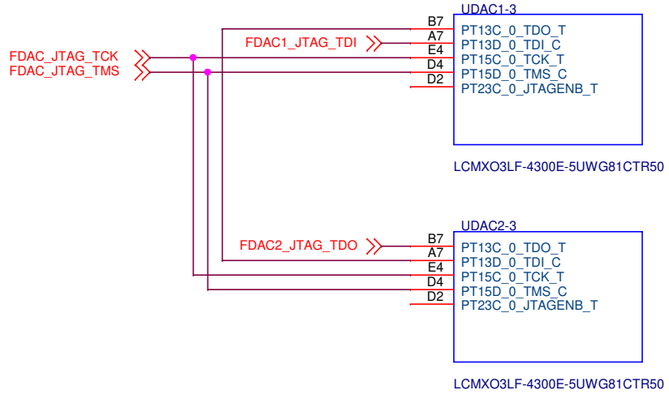
PWM_IN[32..1] <<< PWM_IN[32..1]

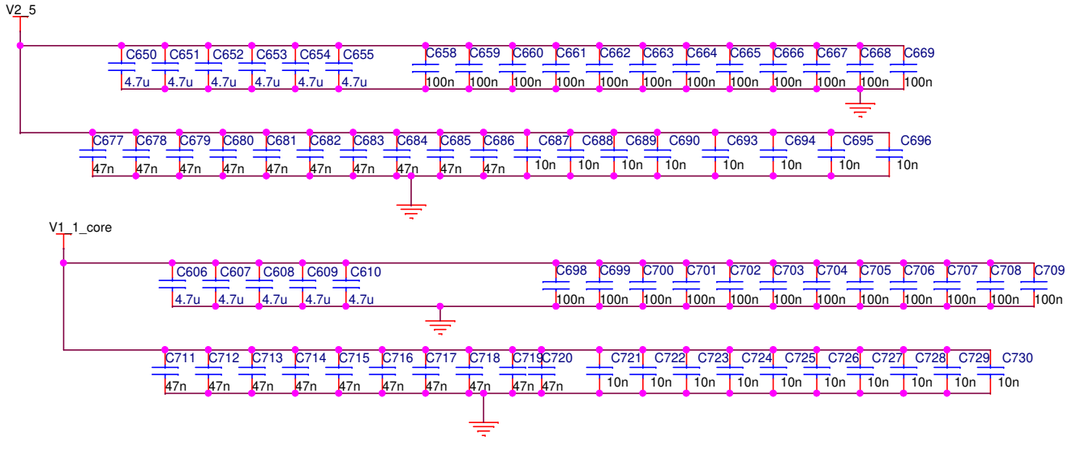












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DAC_FPGA

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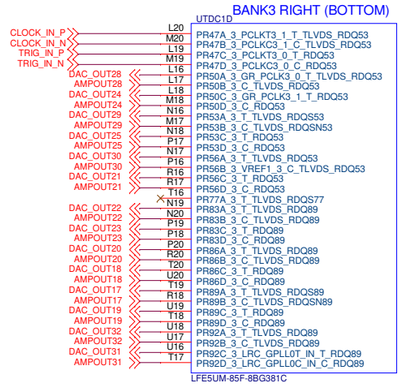
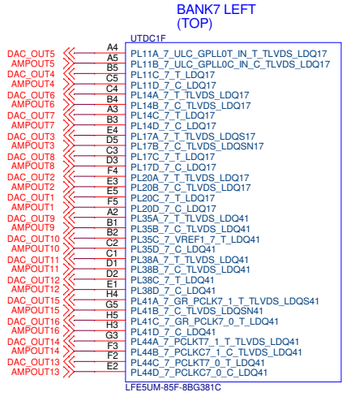
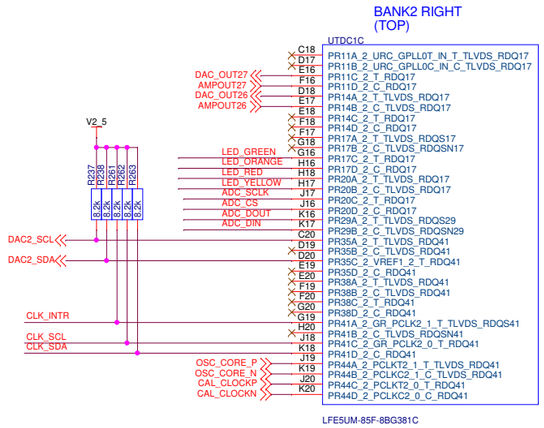
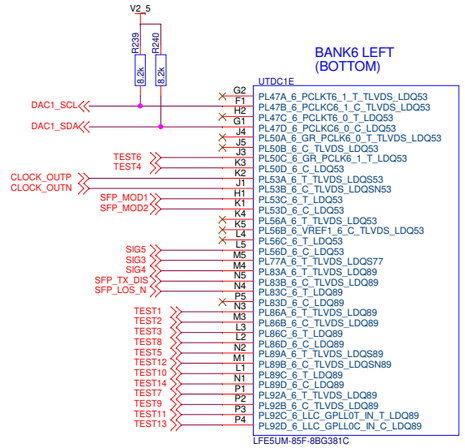
Modified: Tuesday, March 23, 2021 | Size: A3 | Page: 2 / 9
Designer: M.Traxler | Layouter: H.Kavan

Bank 0,1,4,8: no true LVDS inputs
Bank 2,3,6,7: LVDS inputs, 50% LVDS outputs





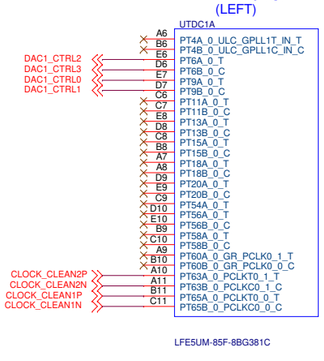


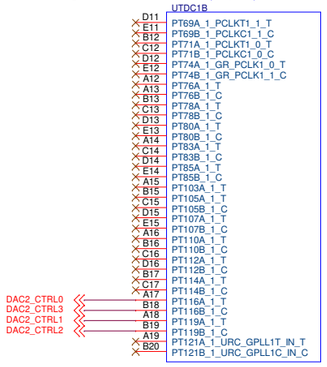


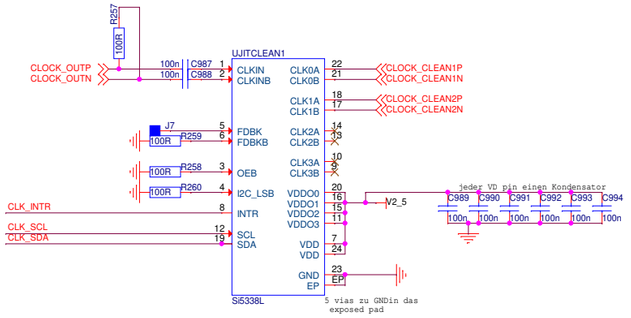
DAC_OUT[32..1] DAC_OUT[32..1]

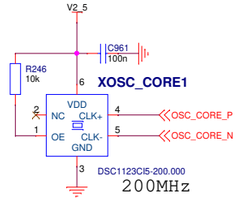
AMPOUT[32..1] AMPOUT[32..1]

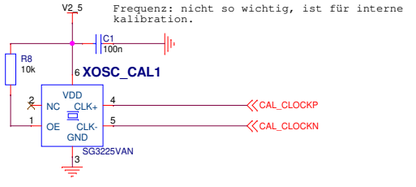
Bank 0,1,4,8: no true LVDS outputs

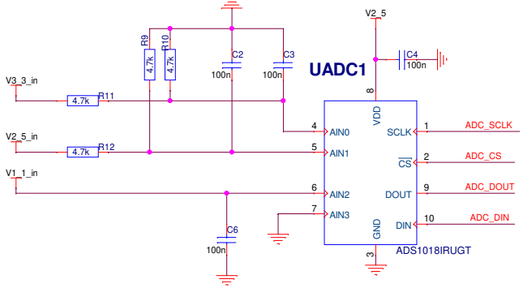


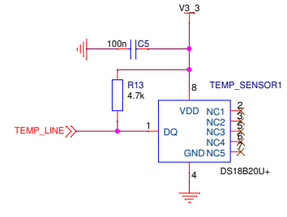


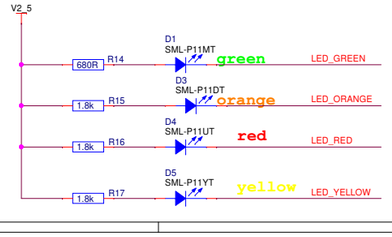












Part No.	Resin Color	Forward voltage V_F		Reverse current I_R		Light wavelength Dominant λD		Brightness I_V		
		Typ. (V)	I_F (mA)	Max. (µA)	V_R (V)	Typ. (nm)	I_F (mA)	Min. (mcd)	Typ. (mcd)	I_F (mA)
SML-P11MT	Transparent Colorless	1.9				569		0.63	2.1	
SML-P11YT		1.9				586		2.5	7.6	
SML-P11DT		1.8	1	100	4	605	1	2.5	7.3	1
SML-P11UT		1.8				621		1.6	5.5	
SML-P11VT		1.8				626		1.0	3.6	

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FPGA

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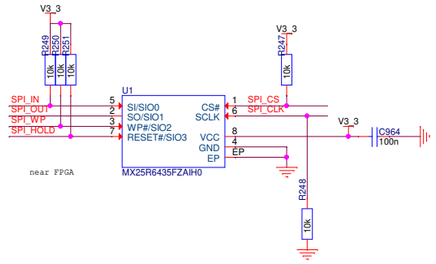
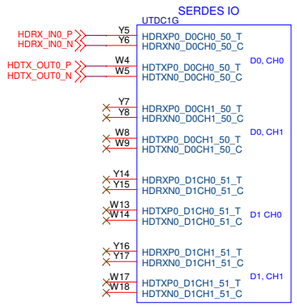
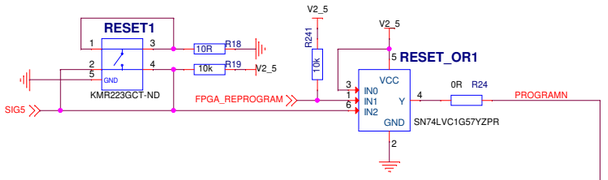
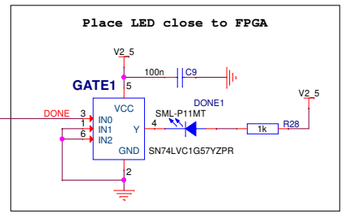
Modified: Tuesday, March 23, 2021	Size: A2 Page: 3 / 9
Designer: M.Traxler	Layouter: H.Kayan



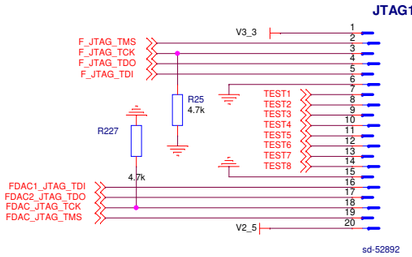


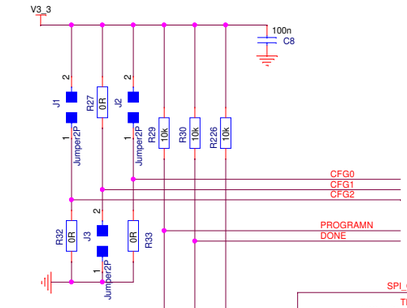
unused serdes channels can be left unpowered and
input signals left floating.
VCCA has always to be powered.

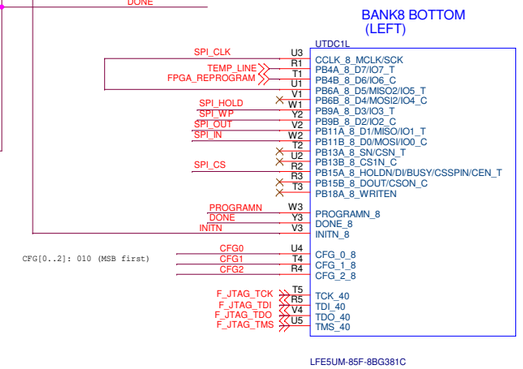




Place JTAG connector
close to the edge







Am Schluß: Gleichmäßig auf dem Board verteilen.
Alles 0201 (0603 metr.)

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FPGA2

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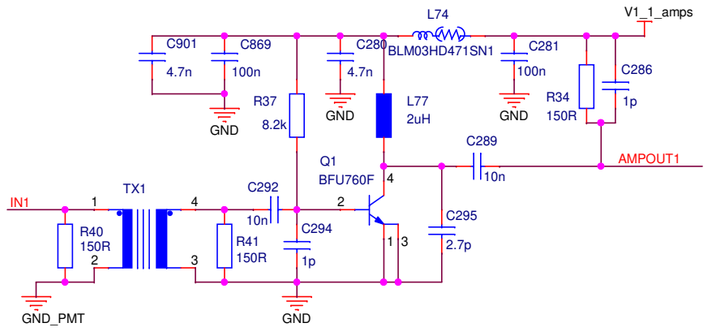
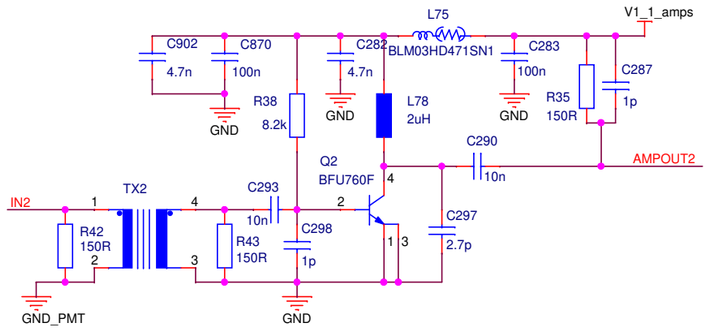
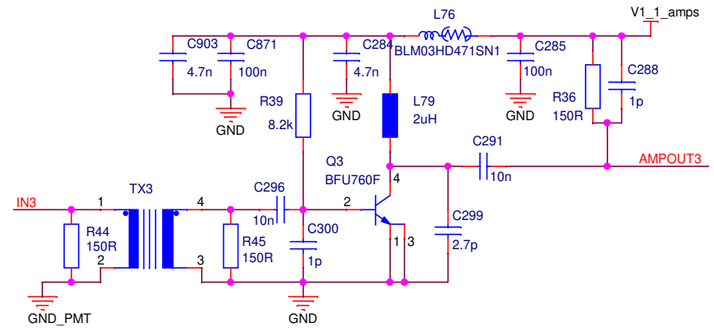
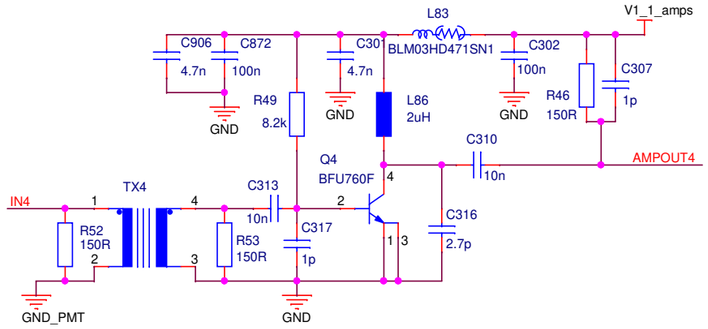
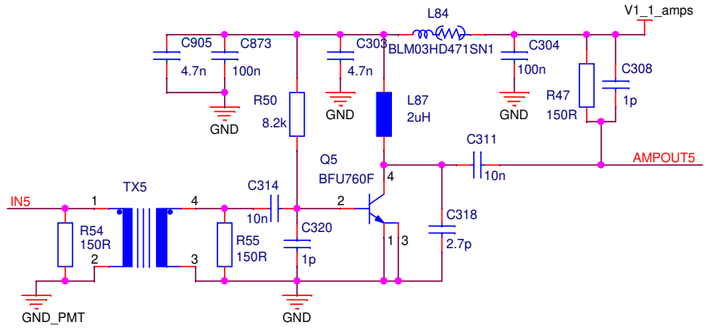
Modified:	Tuesday, March 23, 2021	Size: A2	Page: 4 / 9
Designer:	M.Traxler	Layouter:	H.Kayan

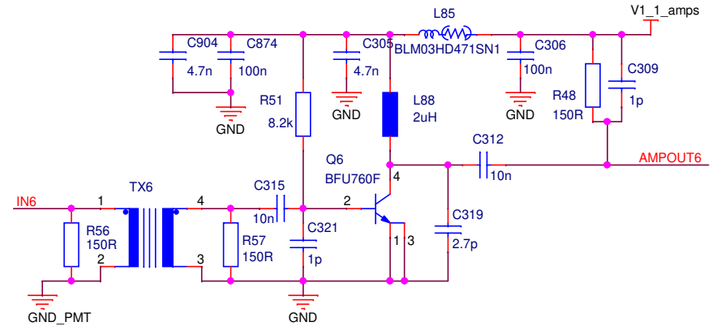


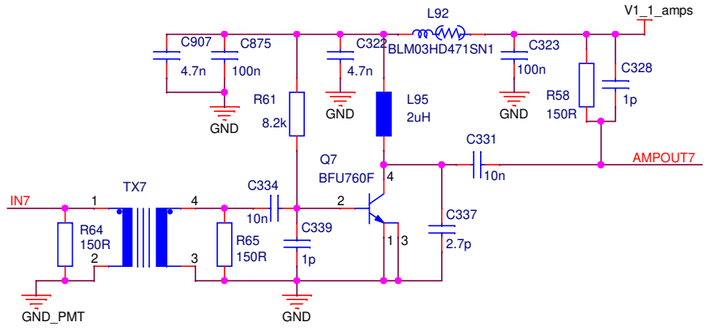


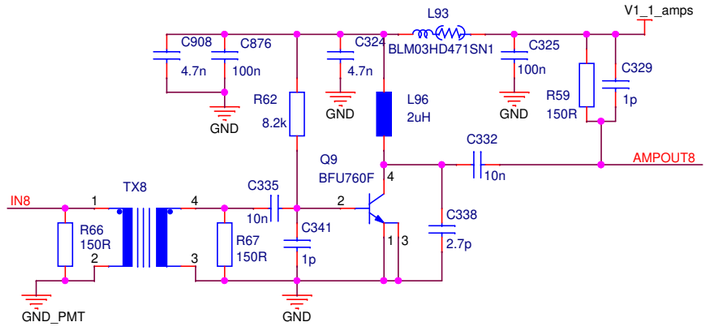


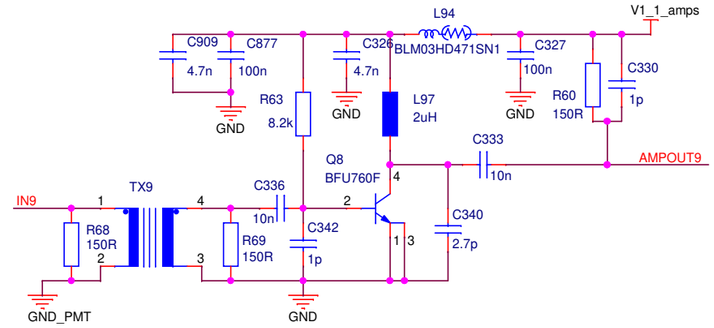


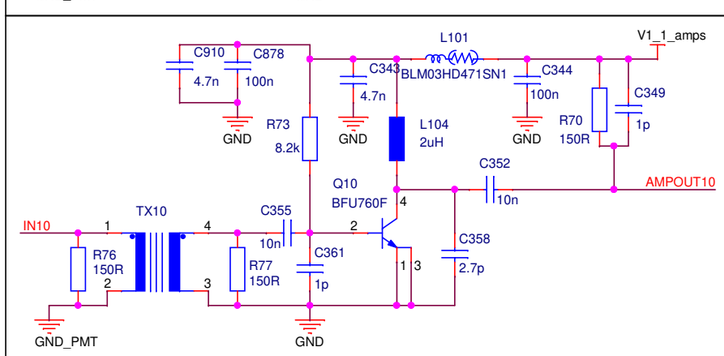


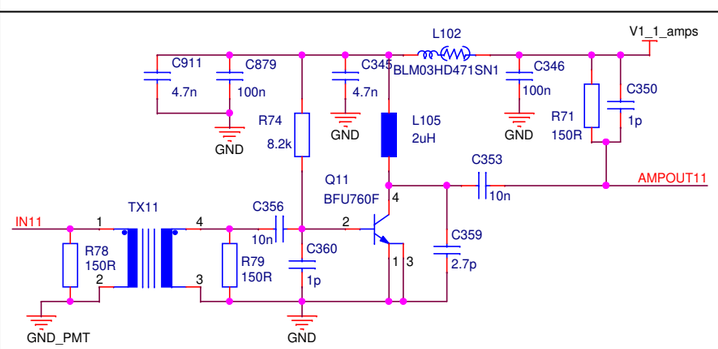


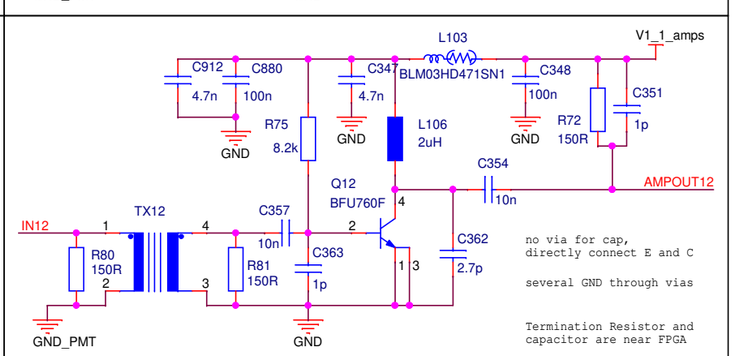












IN[32..1] IN[32..1]

AMPOUT[32..1] AMPOUT[32..1]

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CHANNEL 1-12

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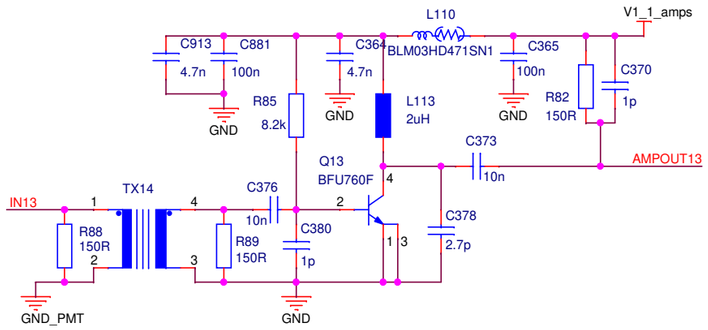
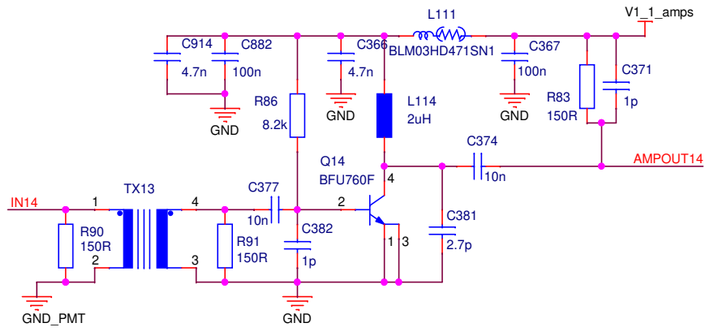
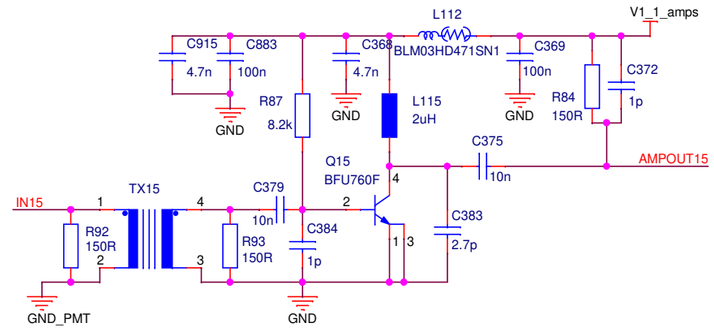
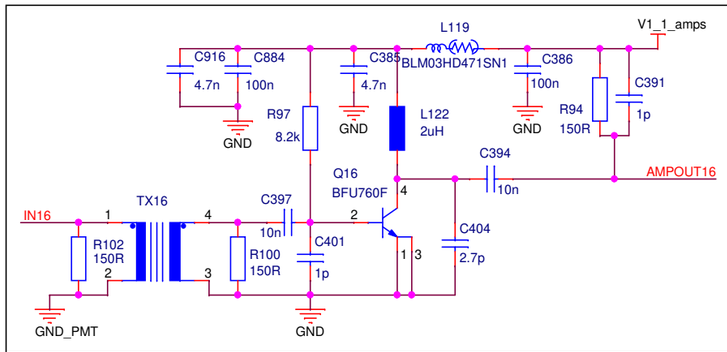
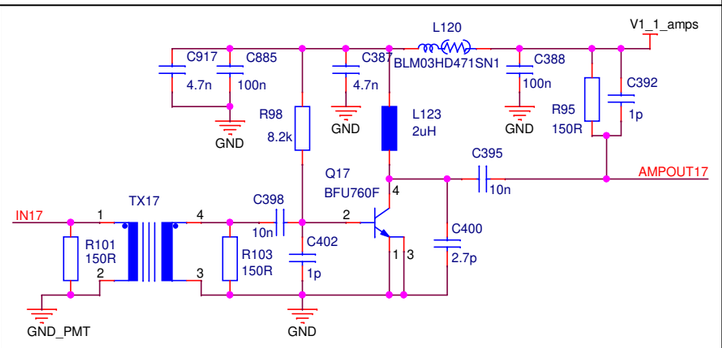
Modified: Tuesday, March 23, 2021	Size: A3	Page: 5 / 9
Designer: M.Traxler	Layouter: H.Kavan	

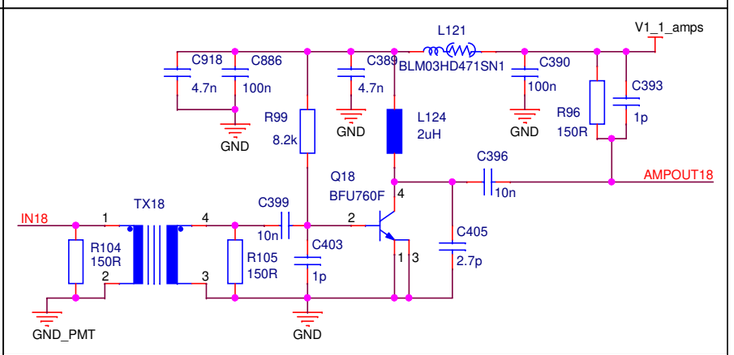


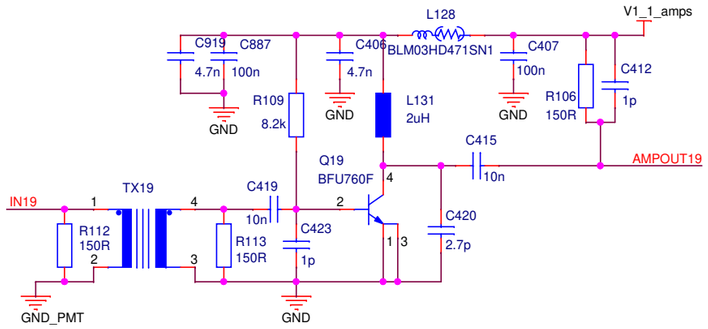


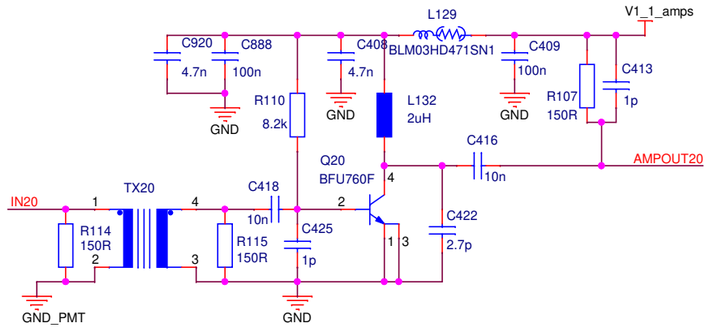


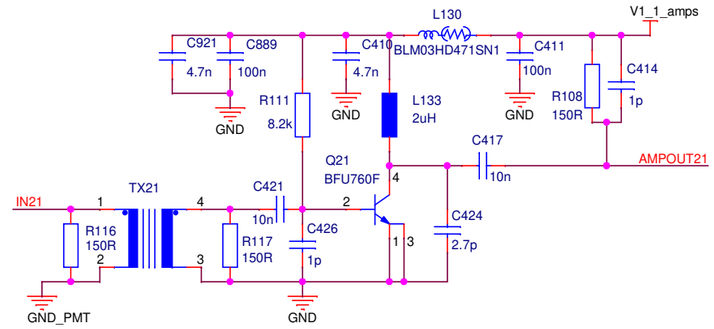


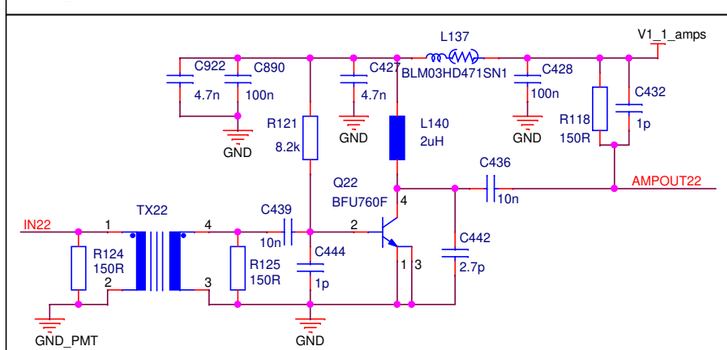


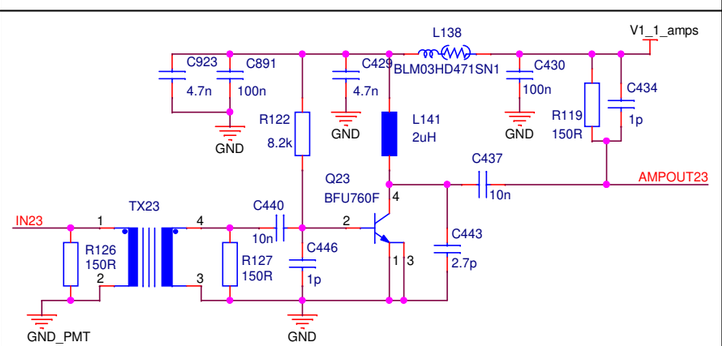


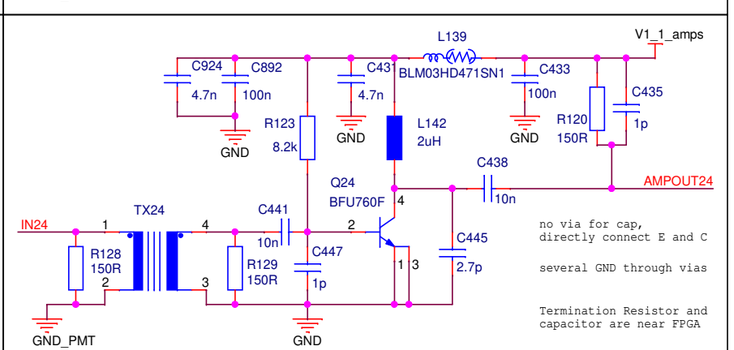












IN[32..1] IN[32..1]

AMPOUT[32..1] AMPOUT[32..1]

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CHANNEL 13-24

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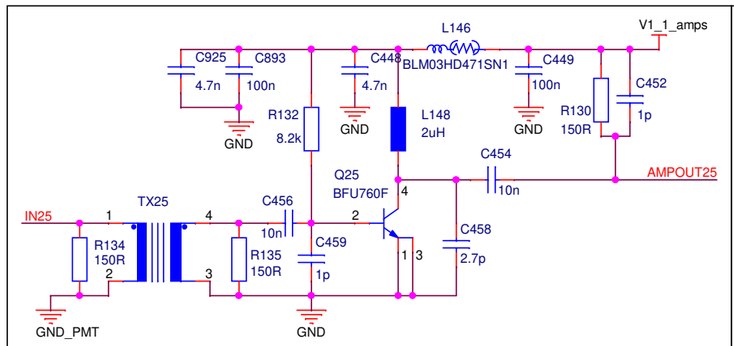
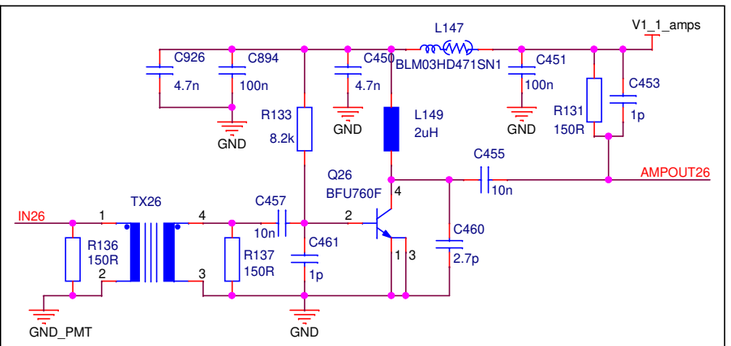
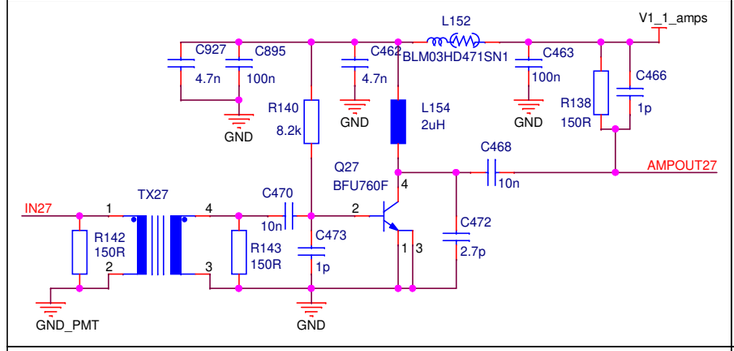
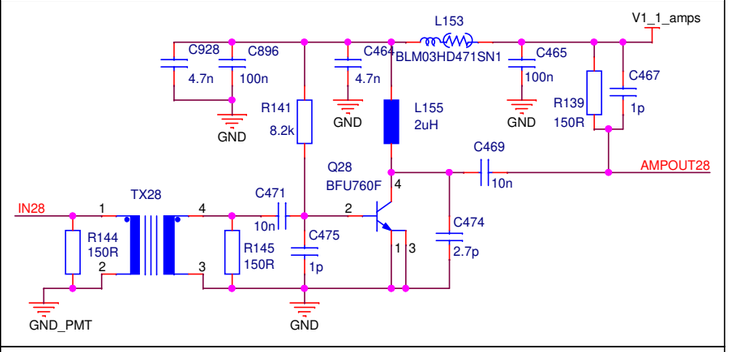
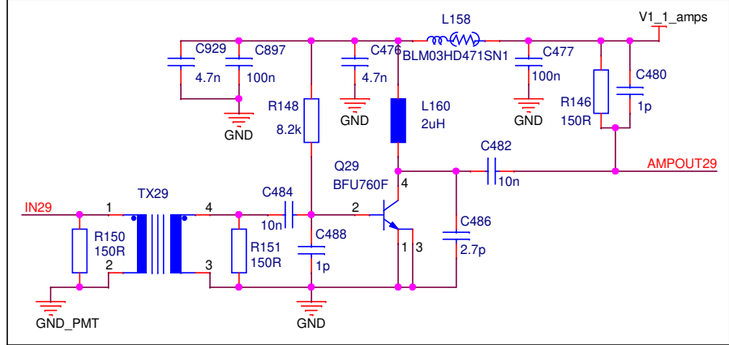
Modified: Tuesday, March 23, 2021	Size: A3	Page: 6 / 9
Designer: M.Traxler	Layouter: H.Kavan	

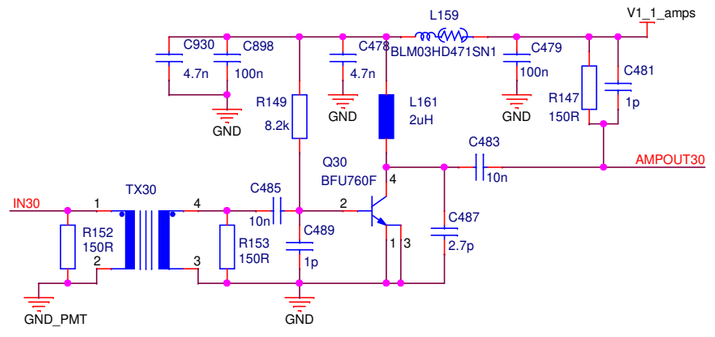


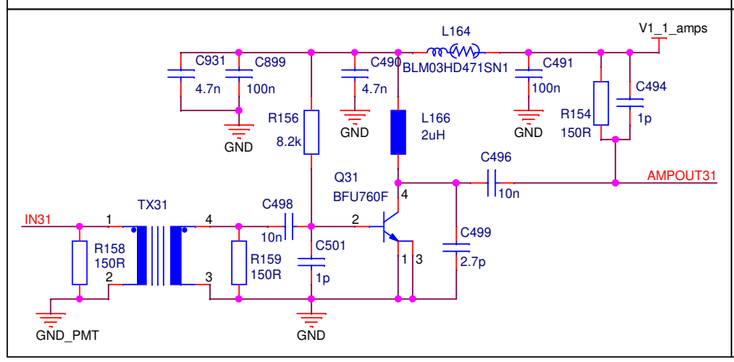


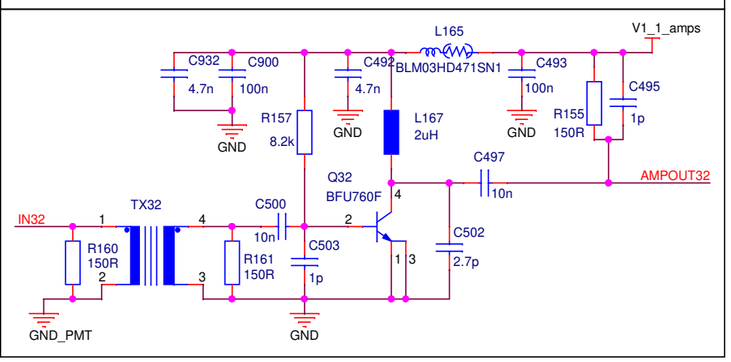












IN[32..1] IN[32..1]

AMPOUT[32..1] AMPOUT[32..1]

no via for cap,
directly connect E and C

several GND through vias

Termination Resistor and
capacitor are near FPGA

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CHANNEL 25-32

Design: K:\GSI\JOB\COME_AND_KISS\DIRICH\DIRICH5S1\DIRICH5S1.DSN
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wire around FPGA, from output side to input side

PWM_IN[32..1] ⟵ PWM_IN[32..1]

DAC_OUT[32..1] ⟶ DAC_OUT[32..1]

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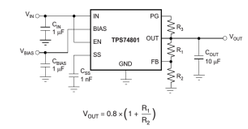
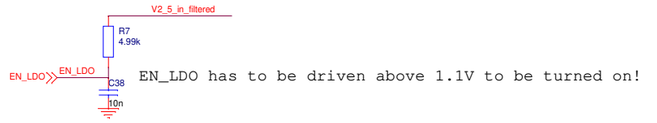
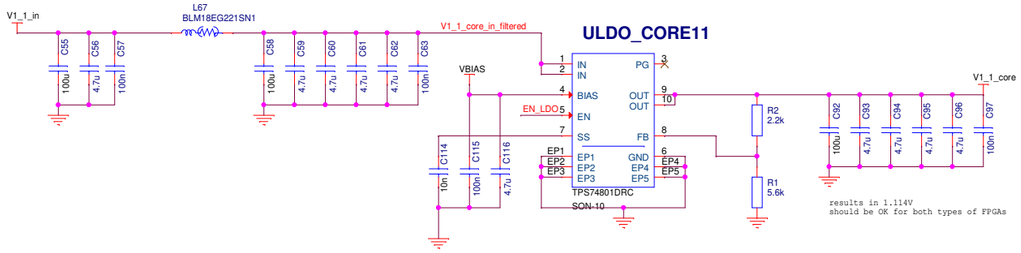
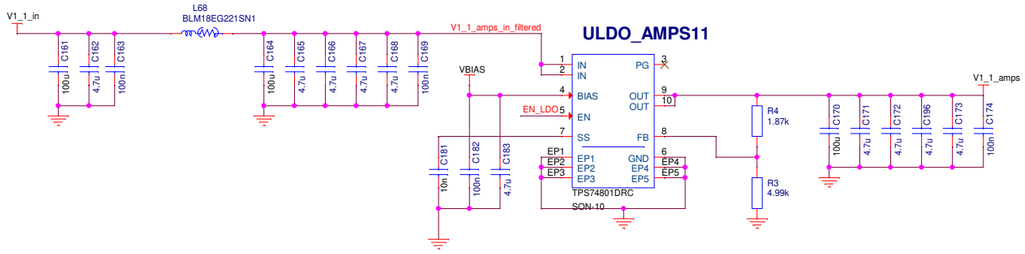
DACs_1-32

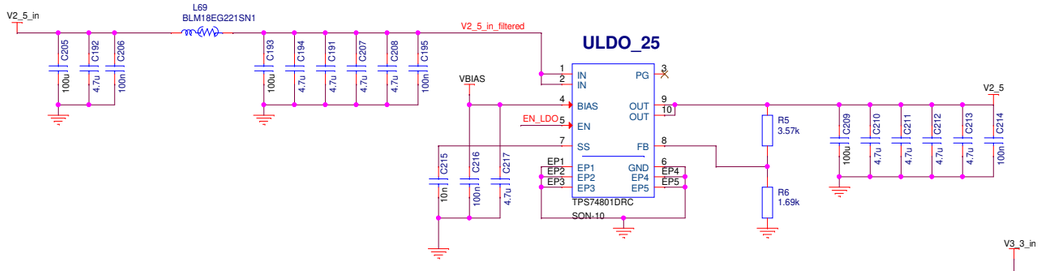
Design: K:\GSIJOB\COME_AND_KISS\DIRICH\DIRICH5S1\DIRICH5S1.DSN		
Modified: Tuesday, March 23, 2021	Size: A3	Page: 8 / 9
Designer: M.Traxler	Layouter: H.Kavan	

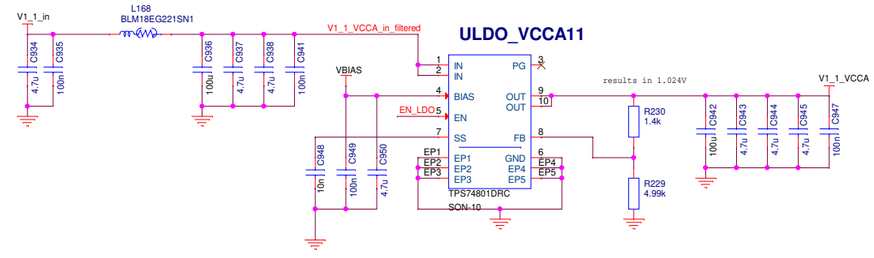


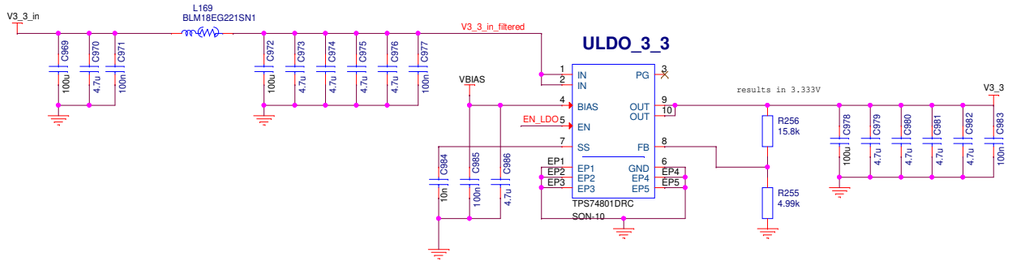


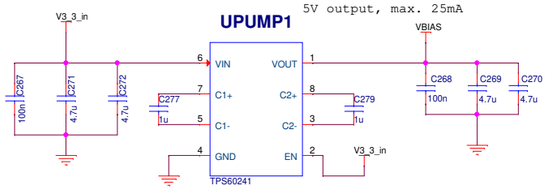


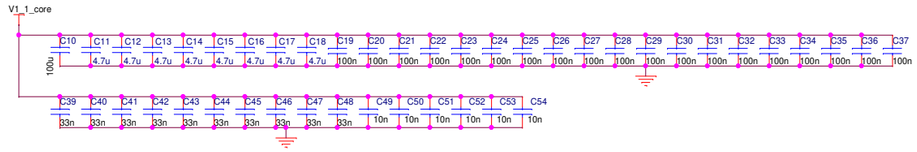


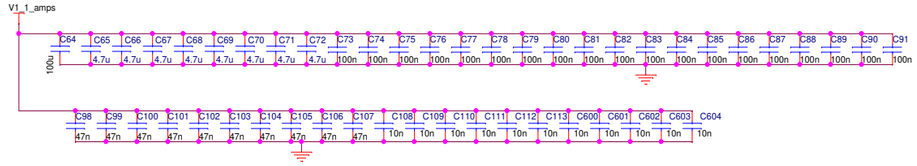


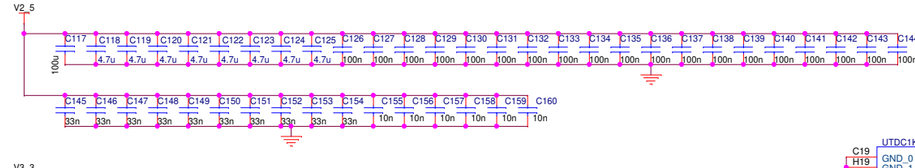


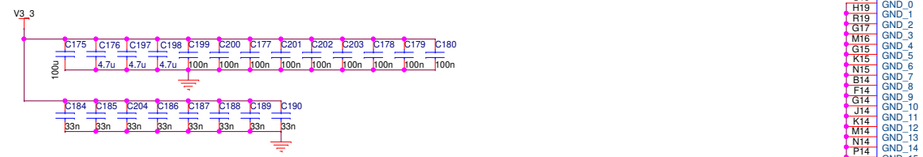


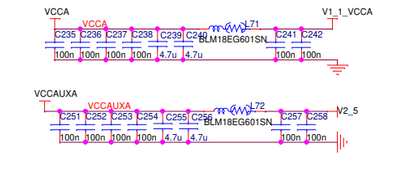


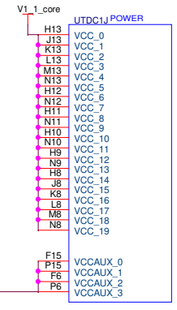


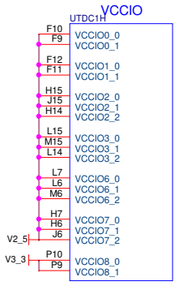


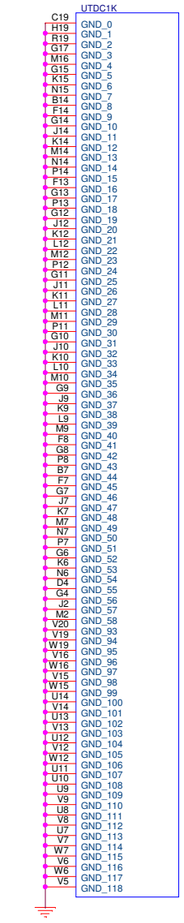


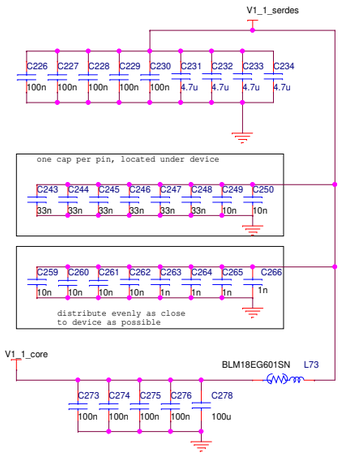


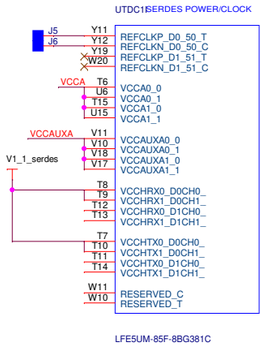












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POWER

Design:	K:\GSI\OB\COME_AND_KISS\DIRICH\DIRICH5S1\DIRICH5S1.DSN
Modified:	Tuesday, March 23, 2021
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Layouter:	H.Kayan