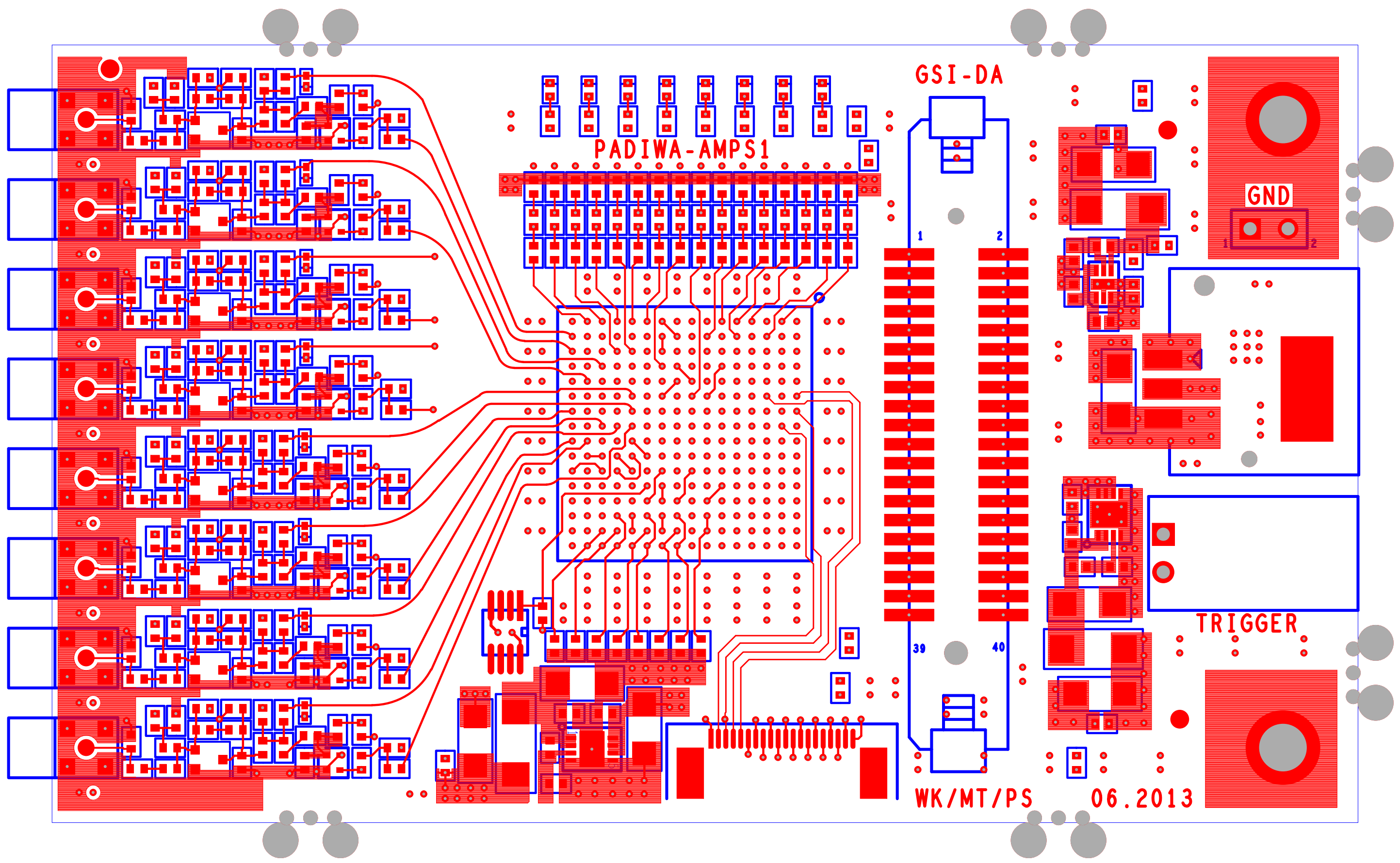
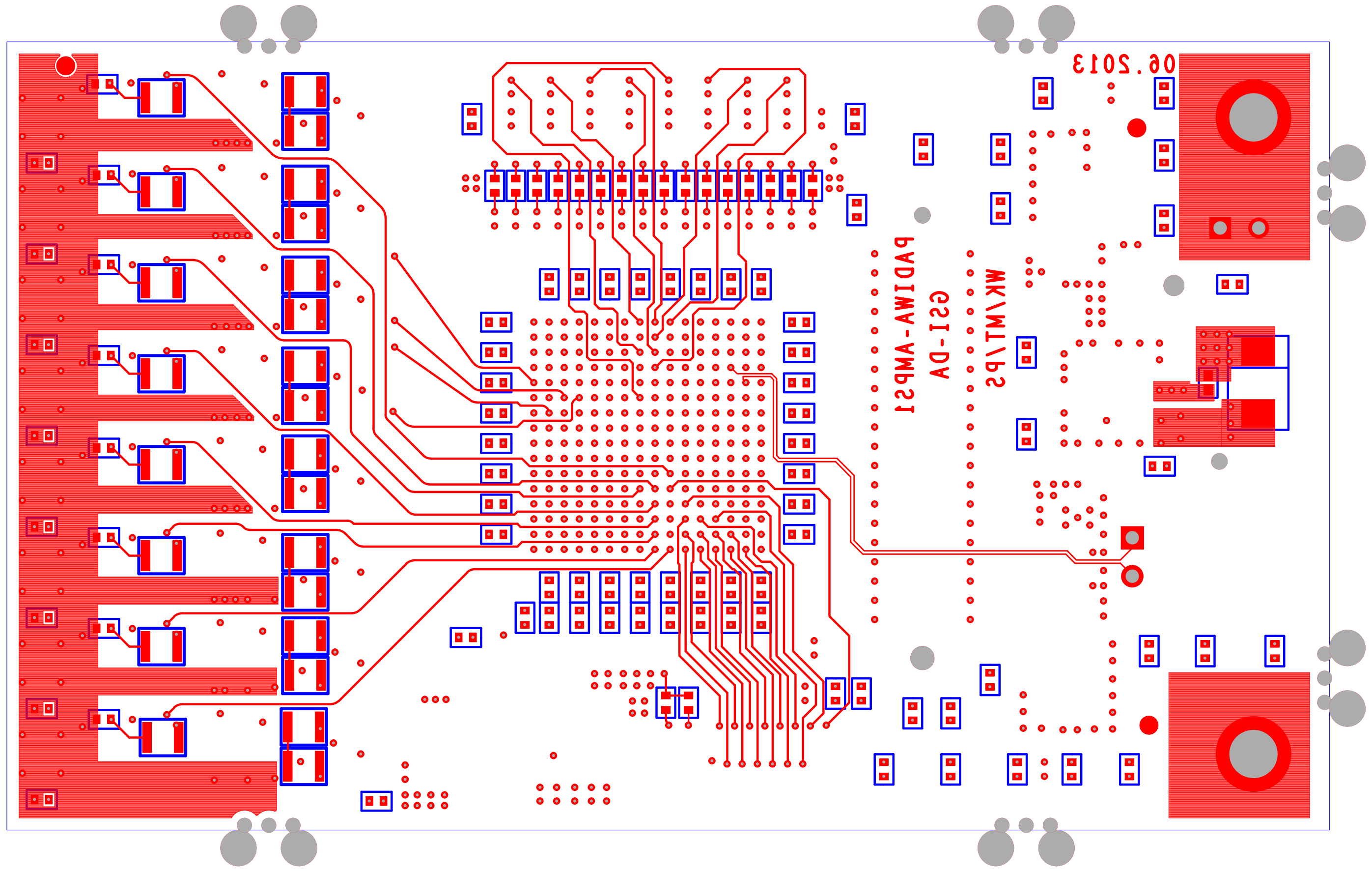


GSI-DA
PADIWA-AMPS1
GND
TRIGGER
WK/MT/PS
06.2013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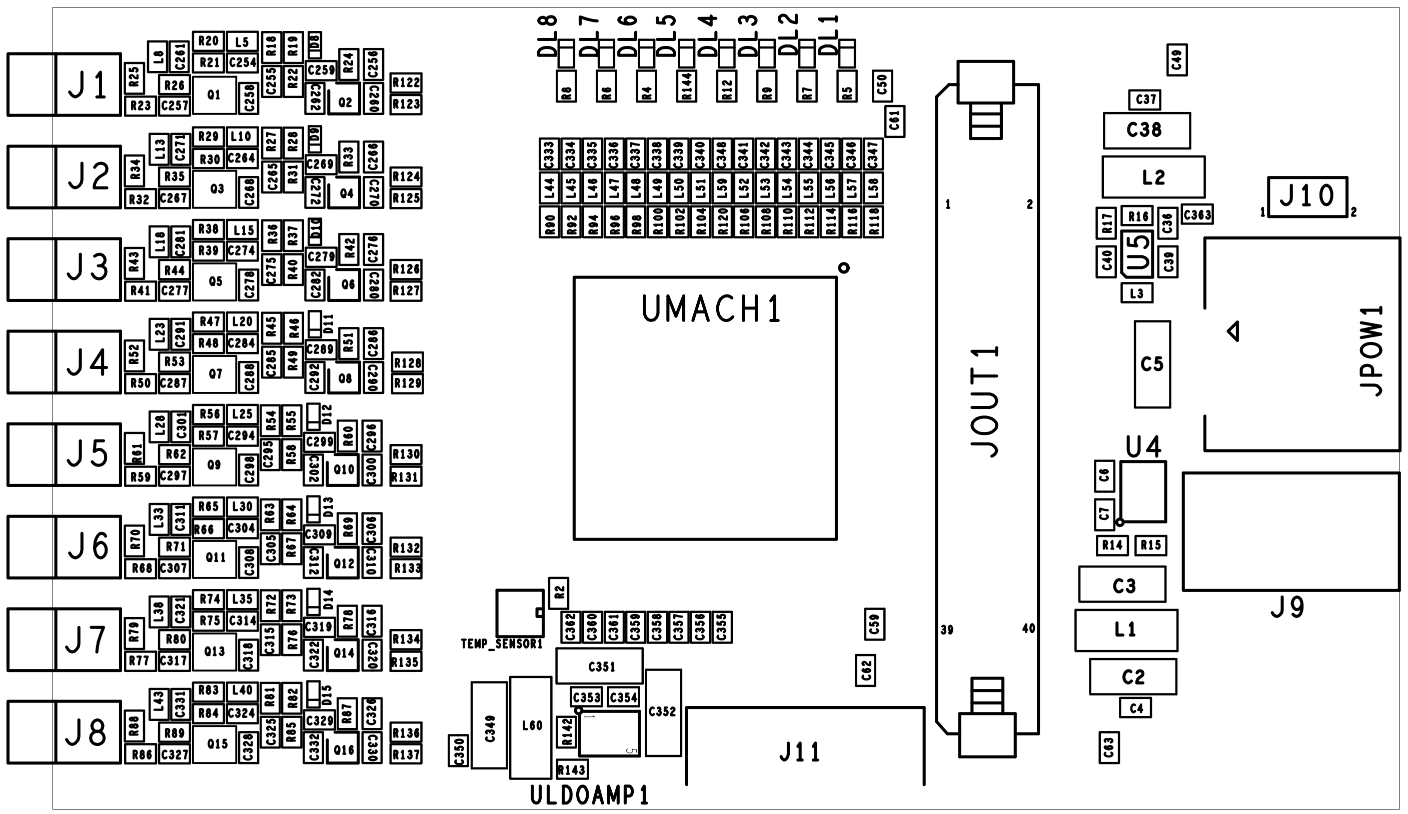
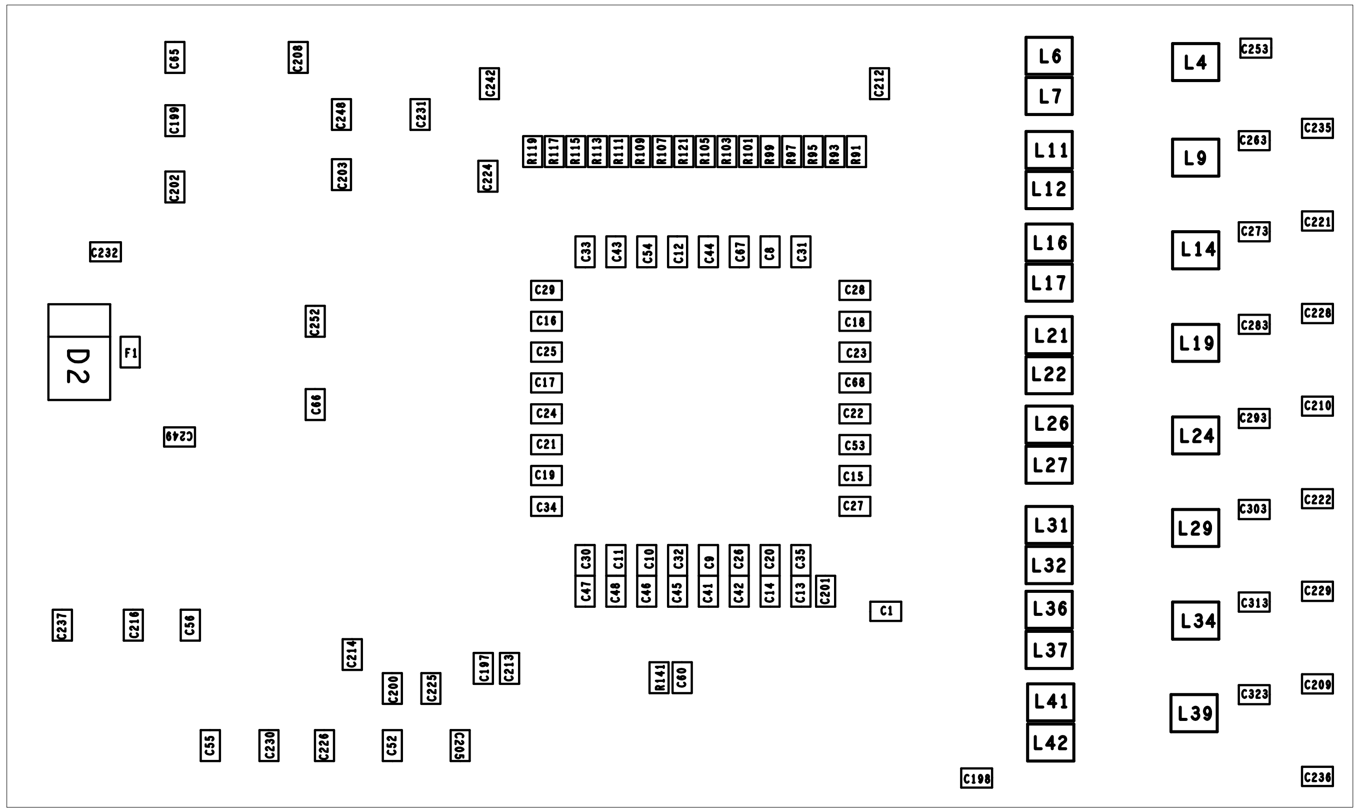
PADIWA-AMPS1
GSI-DA
MW/TM/PS


J1
J2
J3
J4
J5
J6
J7
J8
UMACH1
JOUT1
JPOW1
J9
J10
J11
U4
U5
C38
L2
C5
C3
L1
C2
ULDOAMP1
TEMP_SENSOR1



D2
F1
L4
L6
L7
L9
L11
L12
L14
L16
L17
L19
L21
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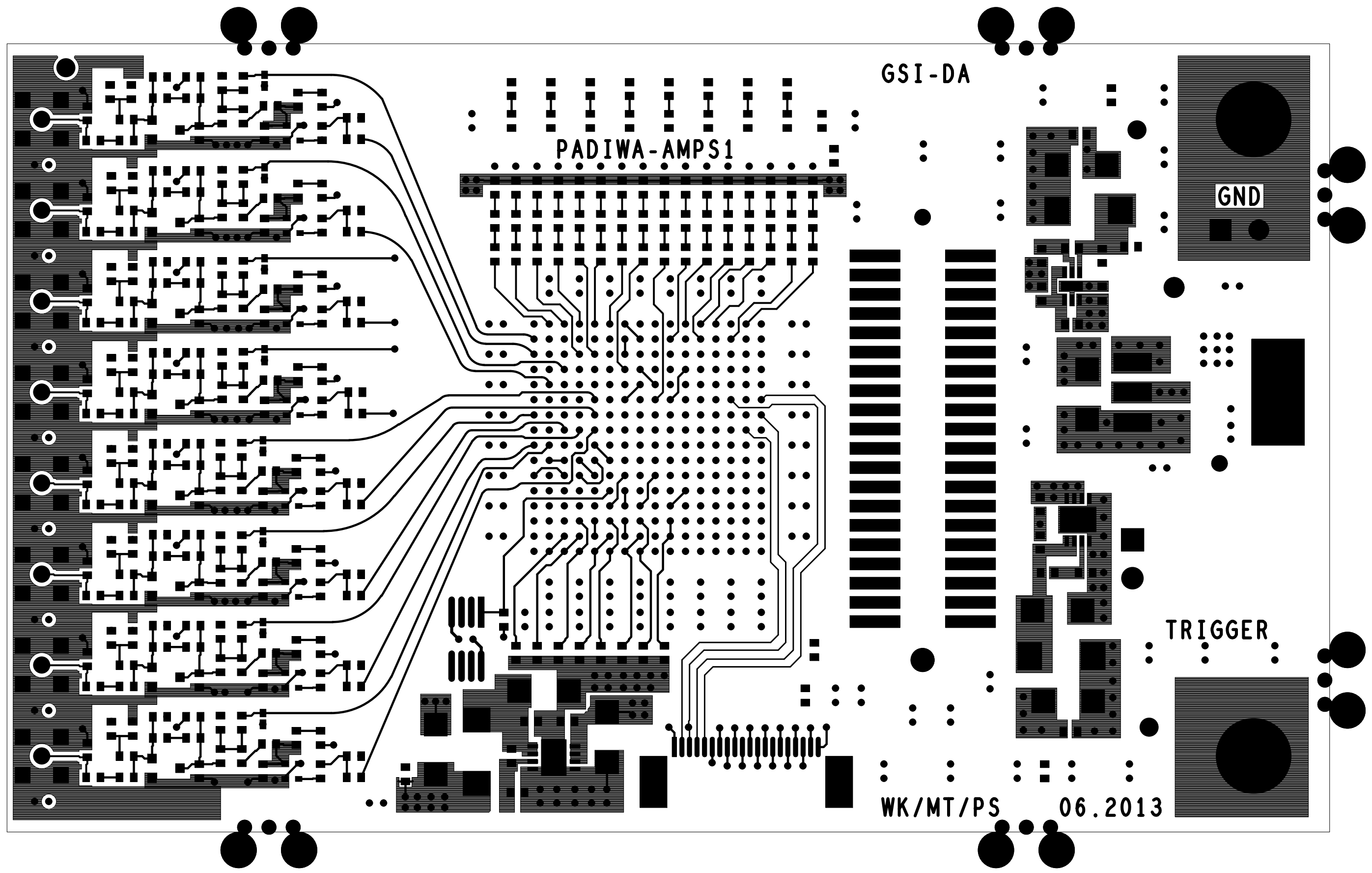
L41
L42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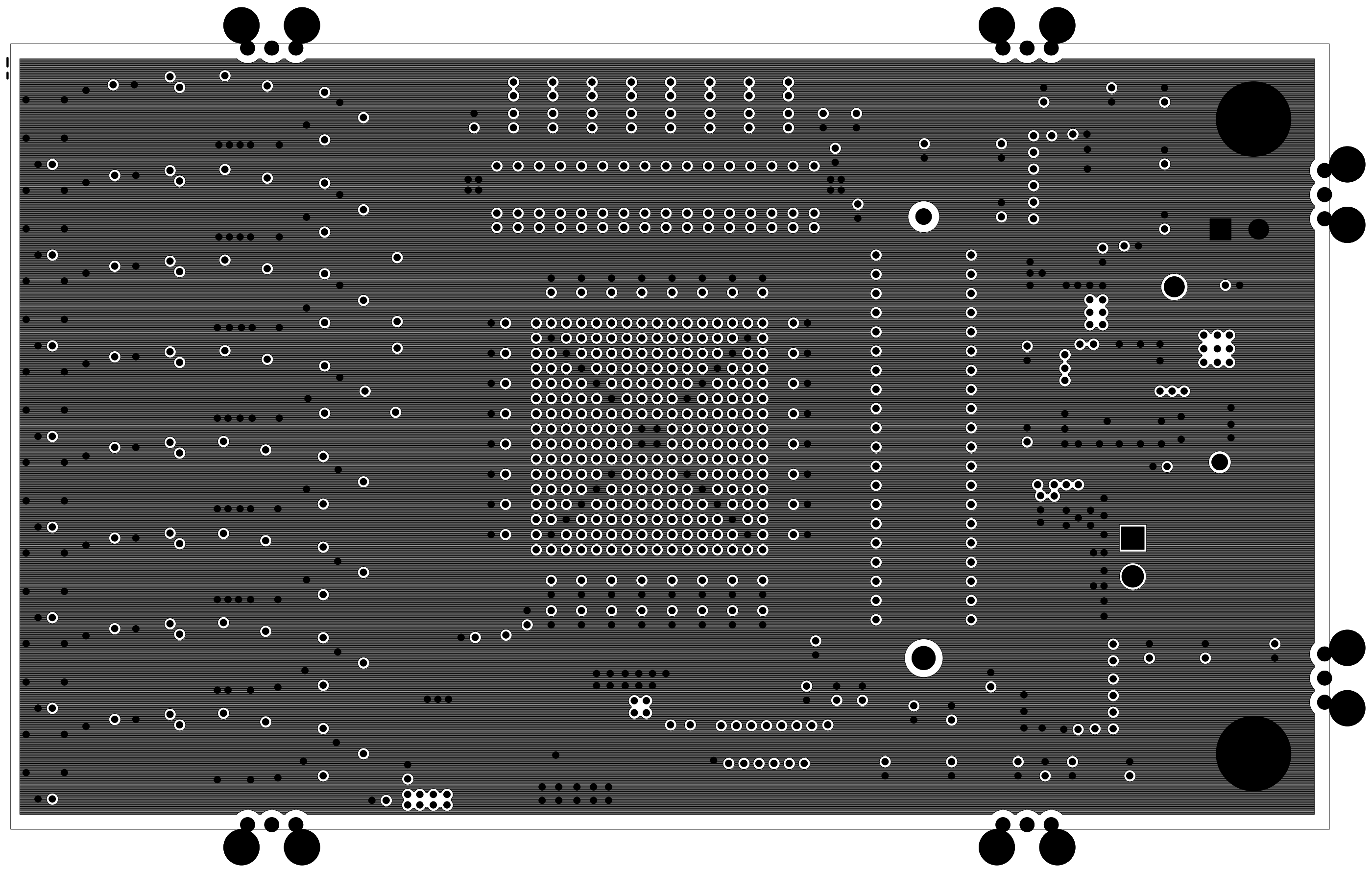
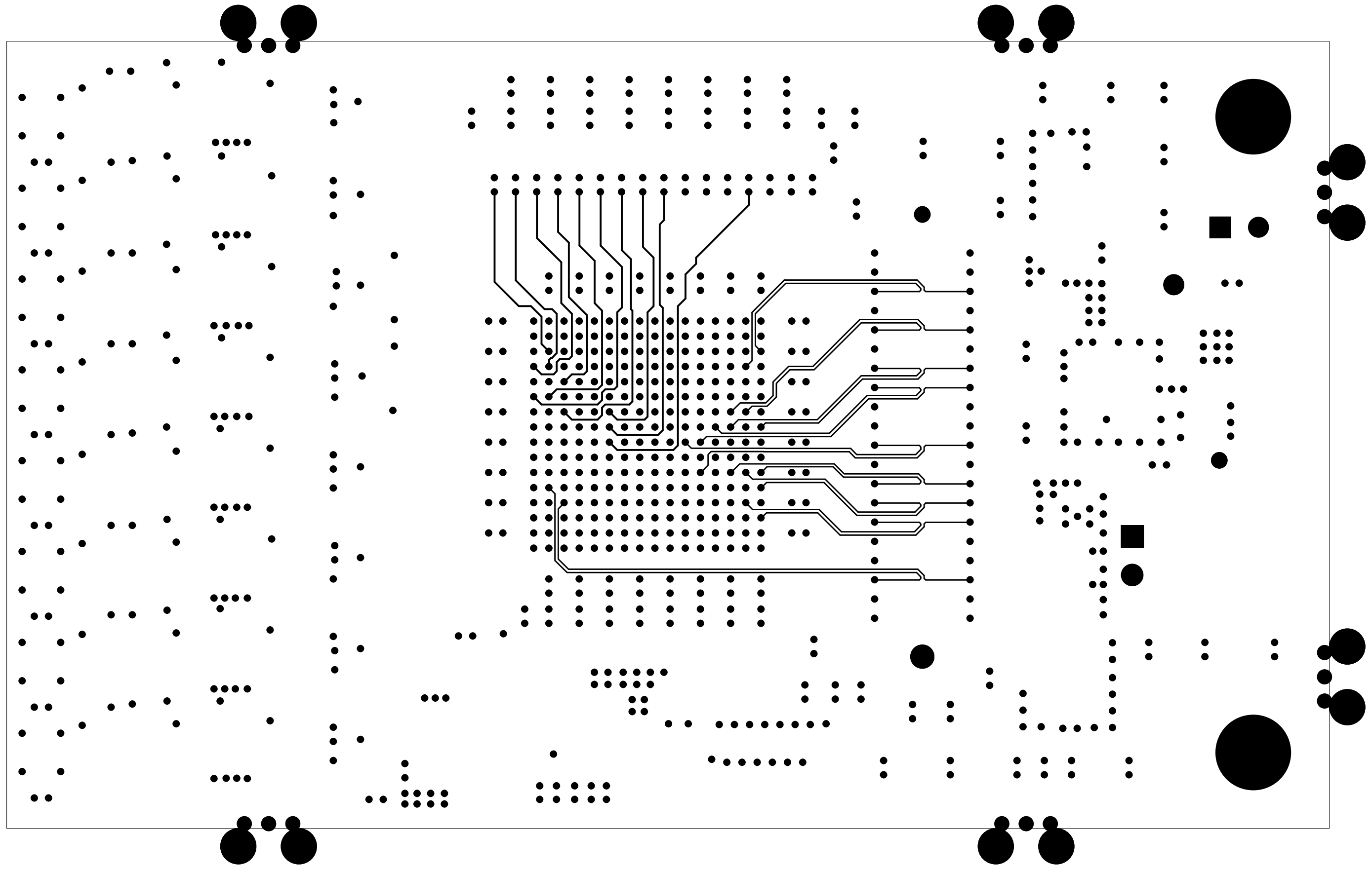
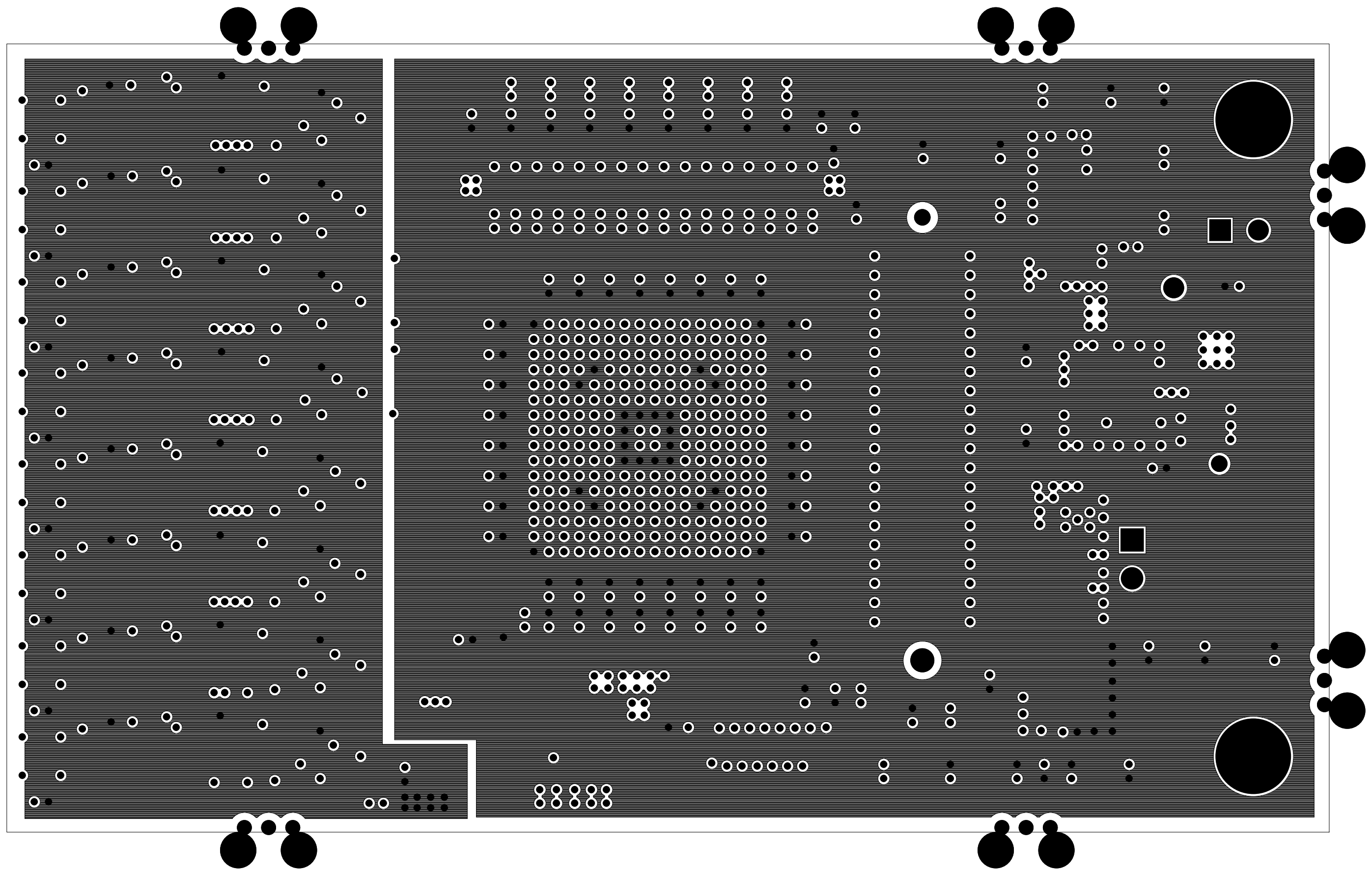
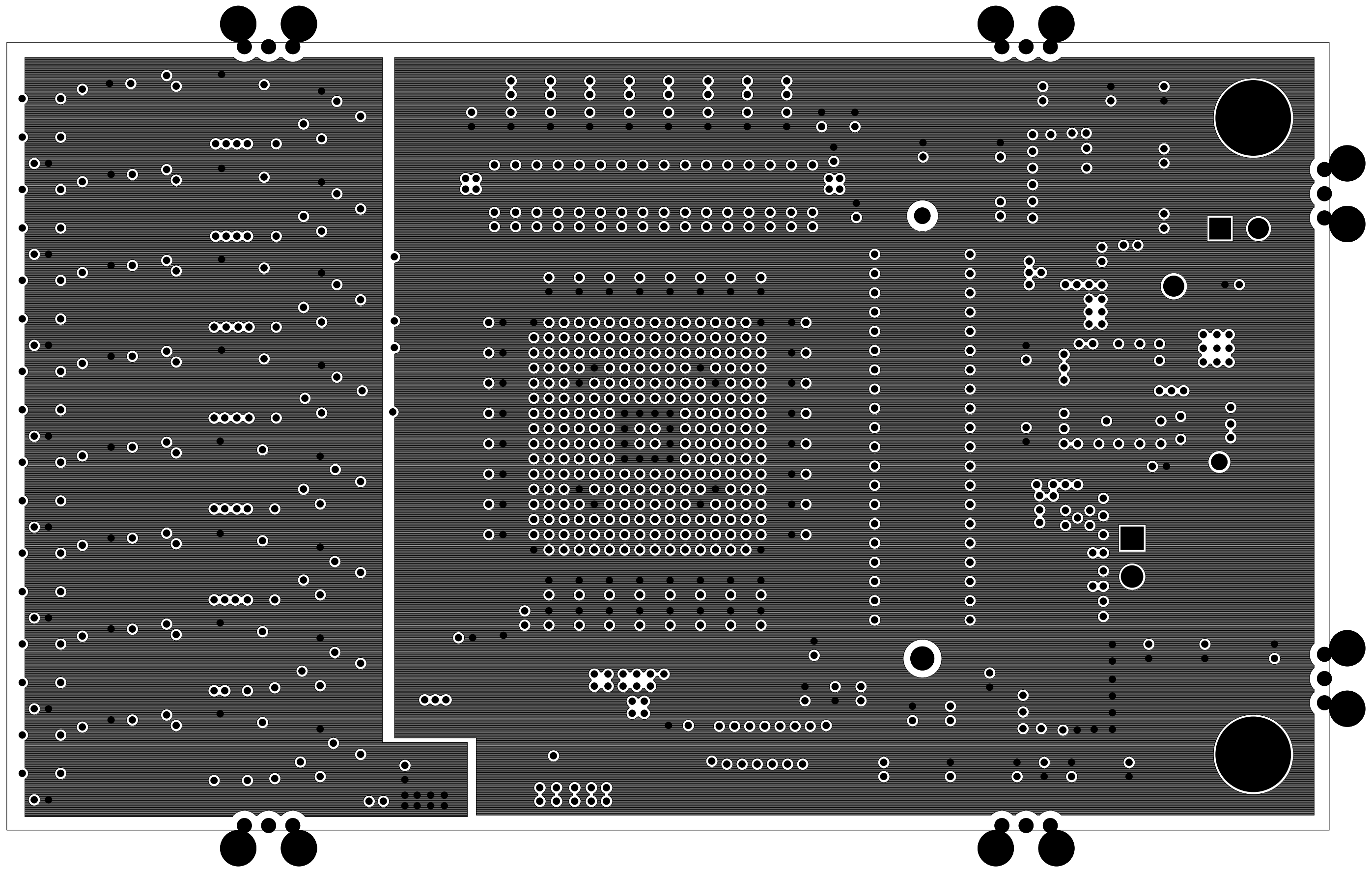
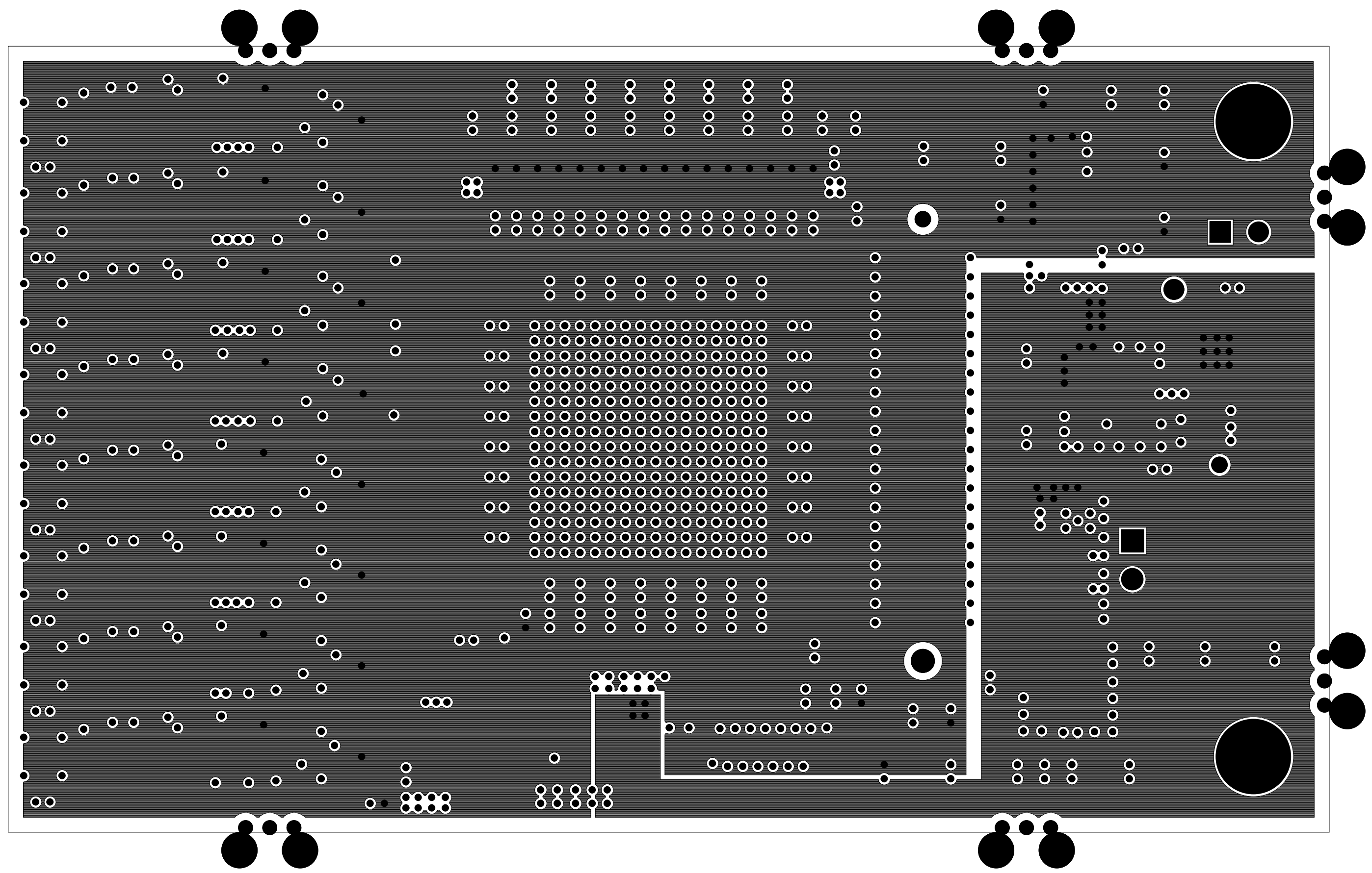
PADIWA-AMPS1
GND
TRIGGER
WK/MT/PS
06.2013

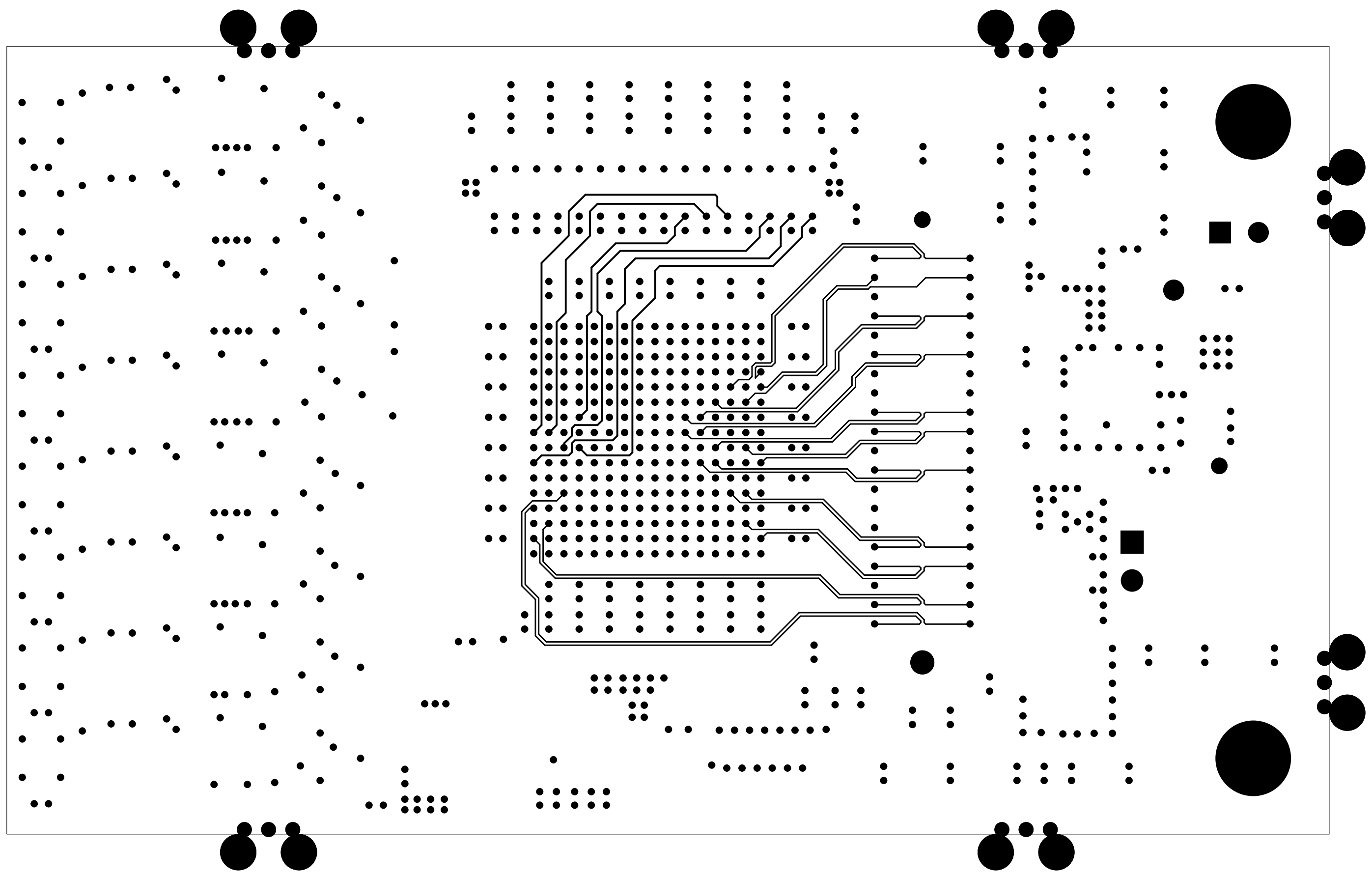


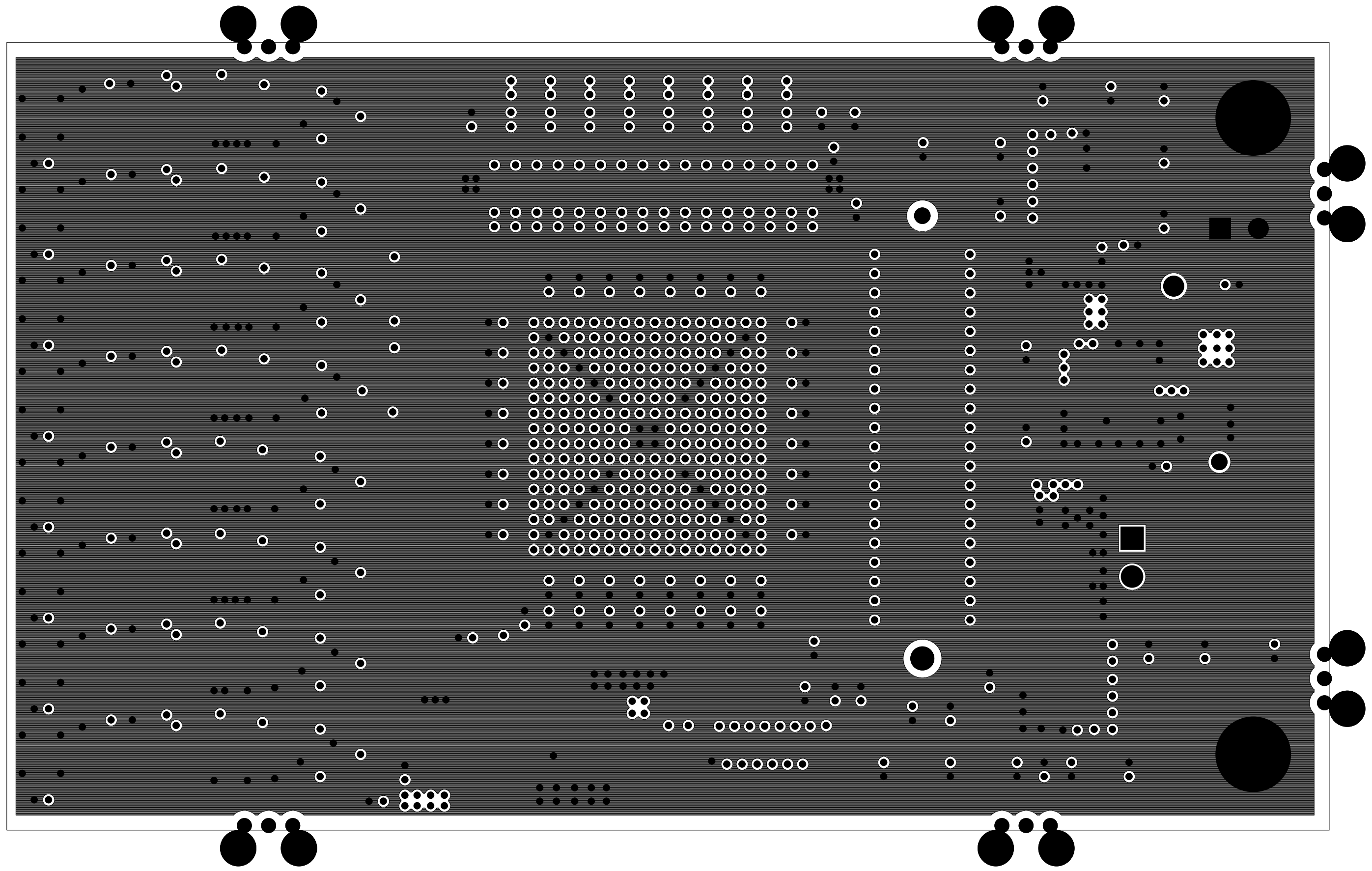


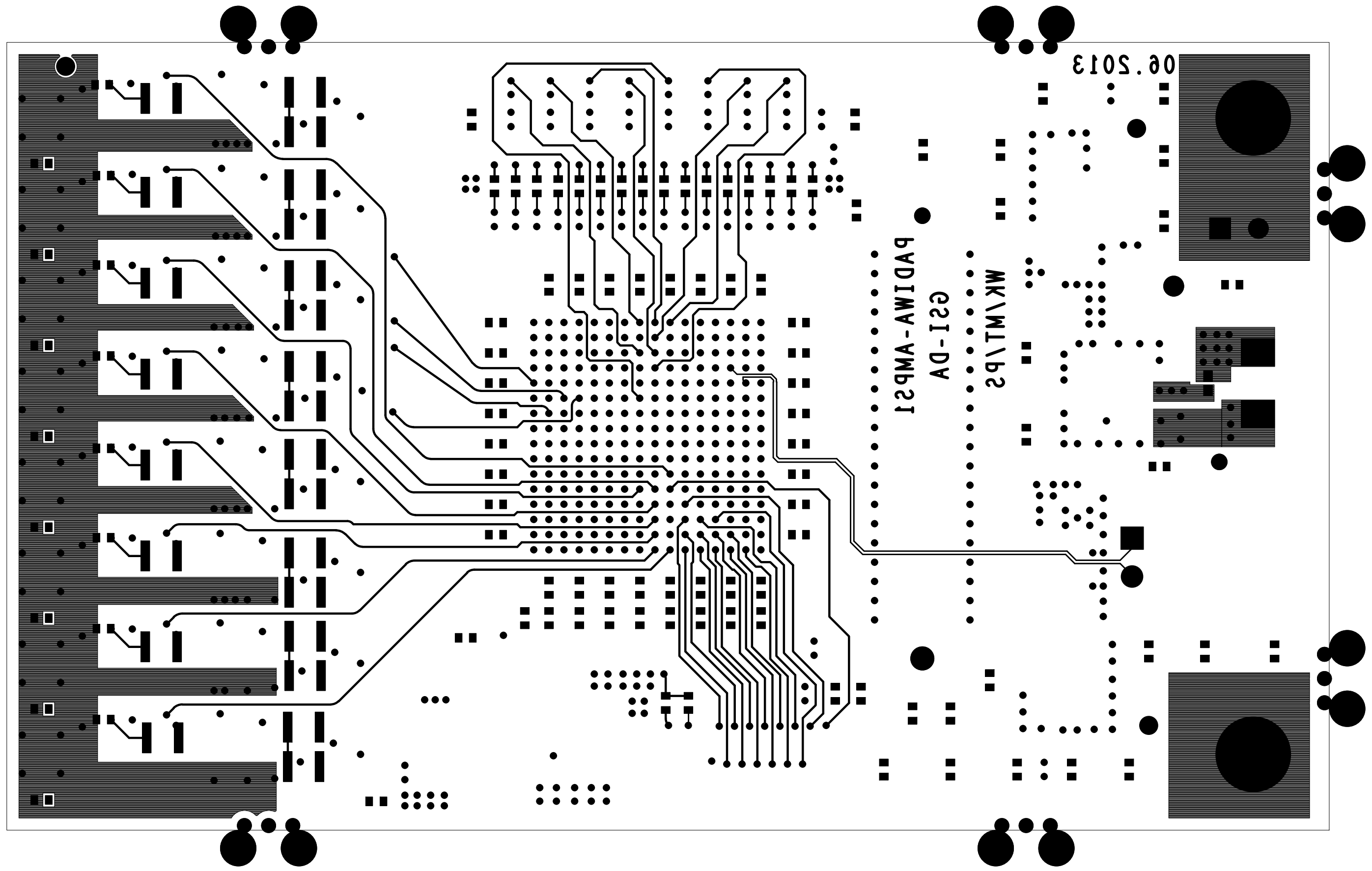








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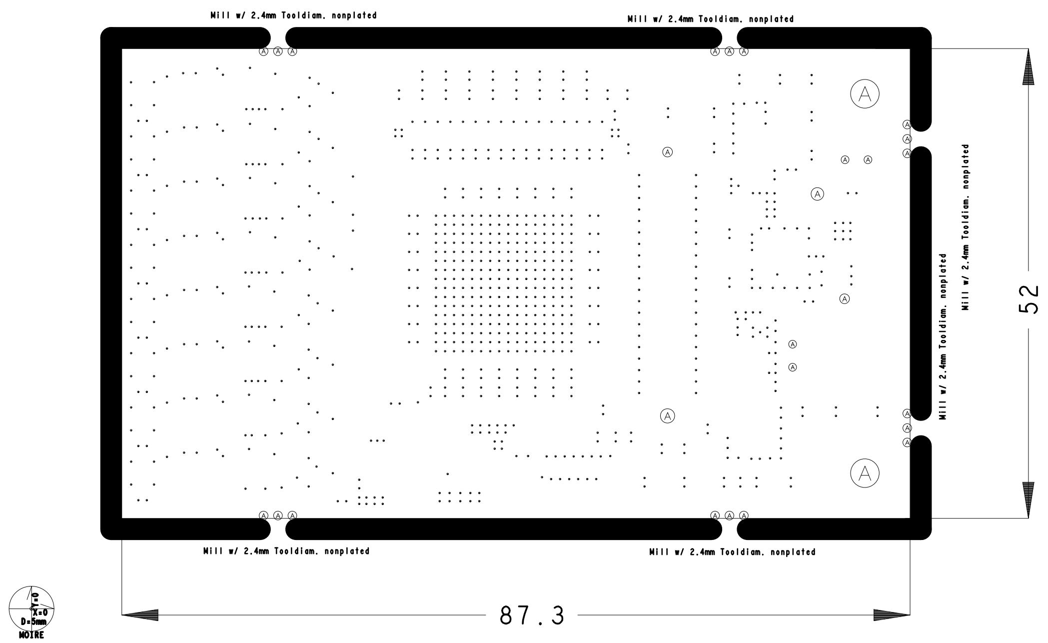
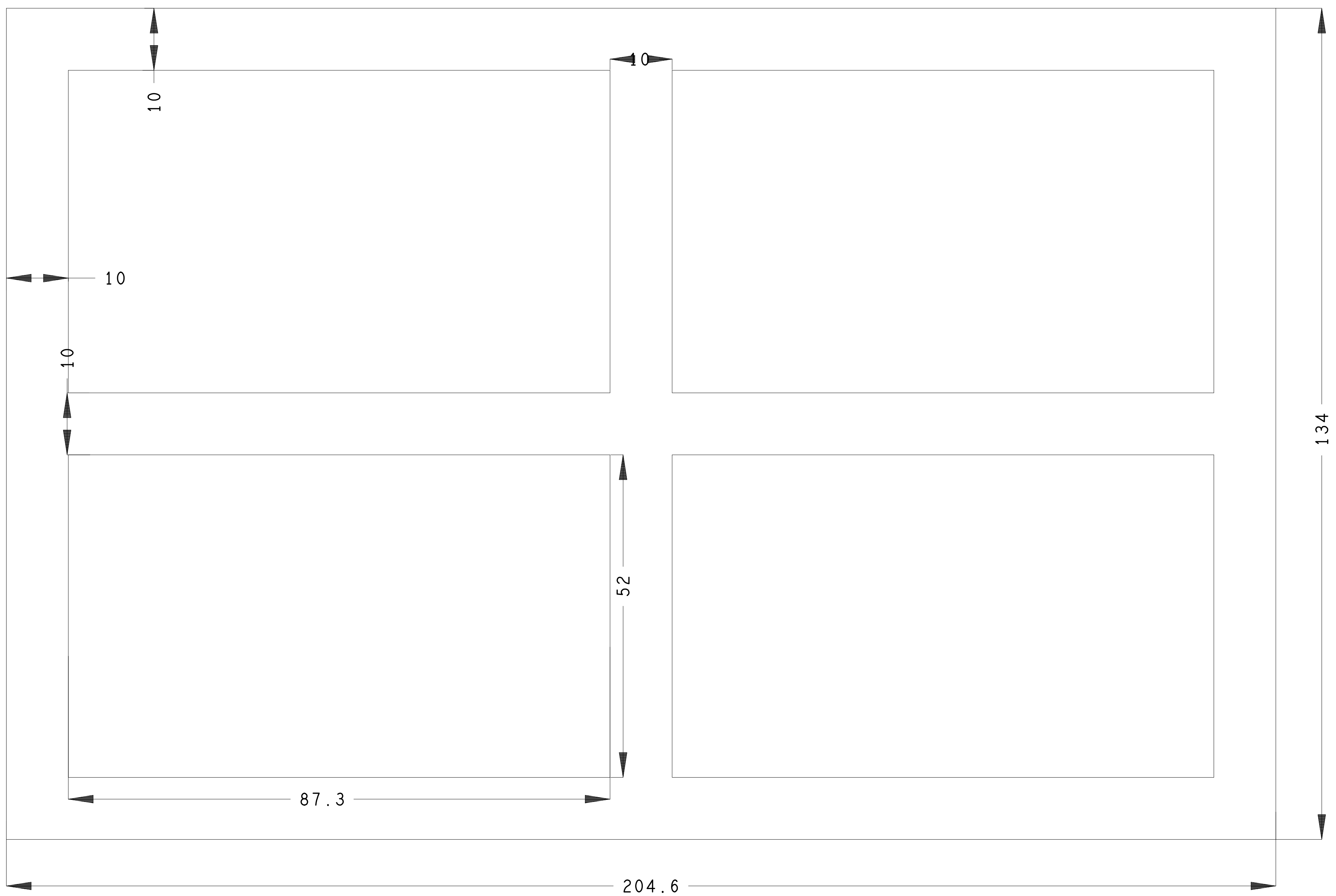
PADIWA-AMPS1
GSI-DA
MK/MT/PS



DRILL CHART: TOP to BOTTOM			
ALL UNITS ARE IN MILLIMETERS			
FIGURE	SIZE	PLATED	QTY
·	0.2	PLATED	879
·	0.4	PLATED	1
A	0.9	PLATED	4
A	3.2	PLATED	2
A	1.0	NON-PLATED	18
A	1.1	NON-PLATED	2
A	1.4	NON-PLATED	1
A	1.6	NON-PLATED	1
A	2.4	NON-PLATED	12
		TOTAL HOLES:	920

Jobname	Date	Designer	Layouter
PADIWA-AMPS1	06.2013	M.Traxler	P.Skott

ckname



Jobname Date Designer Layouter

LAGENAUFBAU (Impedanz)

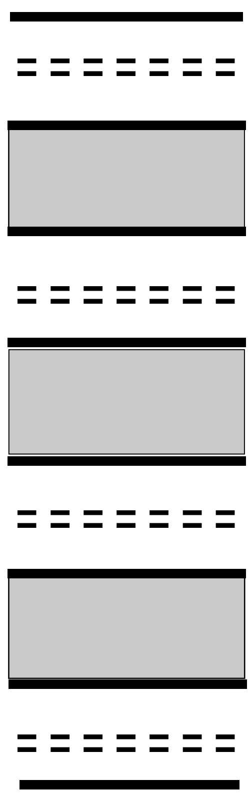
8 - Lagen

Kern: mm Cu / µm

WE-Artikel Nr.:		**8 - Lagen**
KUNDE:	**GSI PADIWA2**	

WÜRTH ELEKTRONIK

LAGENBEZEICHNUNG KUNDE	WE	AUFBAU	BASIS-Material	CU	PREPREG ANZAHL/TYP	ENDDICKE [µm]	KUNDEN-FORDERUNG [µm]
1	TOP/VS		Folie	9 µm	1)	9	
					1x 2113	94	
2	2			18 µm		18	
			0,15 mm			150	
3	3			18 µm		18	
					2x 2116	214	
4	4			18 µm		18	
			0,51 mm			510	
5	5			18 µm		18	
					2x 2116	214	
6	6			18 µm		18	
			0,15 mm			150	
7	7			18 µm		18	
					1x 2113	94	
8	BOT/RS		Folie	9 µm		9	



Imp	Imp.-Lage	LBBR	ISO	ISO z. Masse
Zdiff	L3/L6 = 100,10 Ohm	100µm	120µm	
Zdiffcopl	L3/L6 = 100,30 Ohm	100µm	130µm	150µm
Zo	VS/RS =49,30 Ohm	150 µm		
Zo copl	VS/RS =49,90 Ohm	130µm		150µm

1) Kupferenddicke Außenlagen nach IPC (35µm Forderung)

Material TG 150 hf

Gesamtdicke Material: 1552

Anmerkung: Werte für Prepreg sind Mittelwerte (der genaue Wert ist von den Leiterbildstrukturen abhängig)

						Index	Datum:	Bearbeiter:
MATERIALDICKE:	**1,53**	+/-	0,16	mm				A.Wodke
DICKE über galv. Endoberfläche	1,60	+/-	0,17	mm				
DICKE über LSM incl.galv.-Kupfer	1,64	+/-	0,18	mm			05.12.2012	
Kundenforderung:		+/-		mm	Messstelle:			

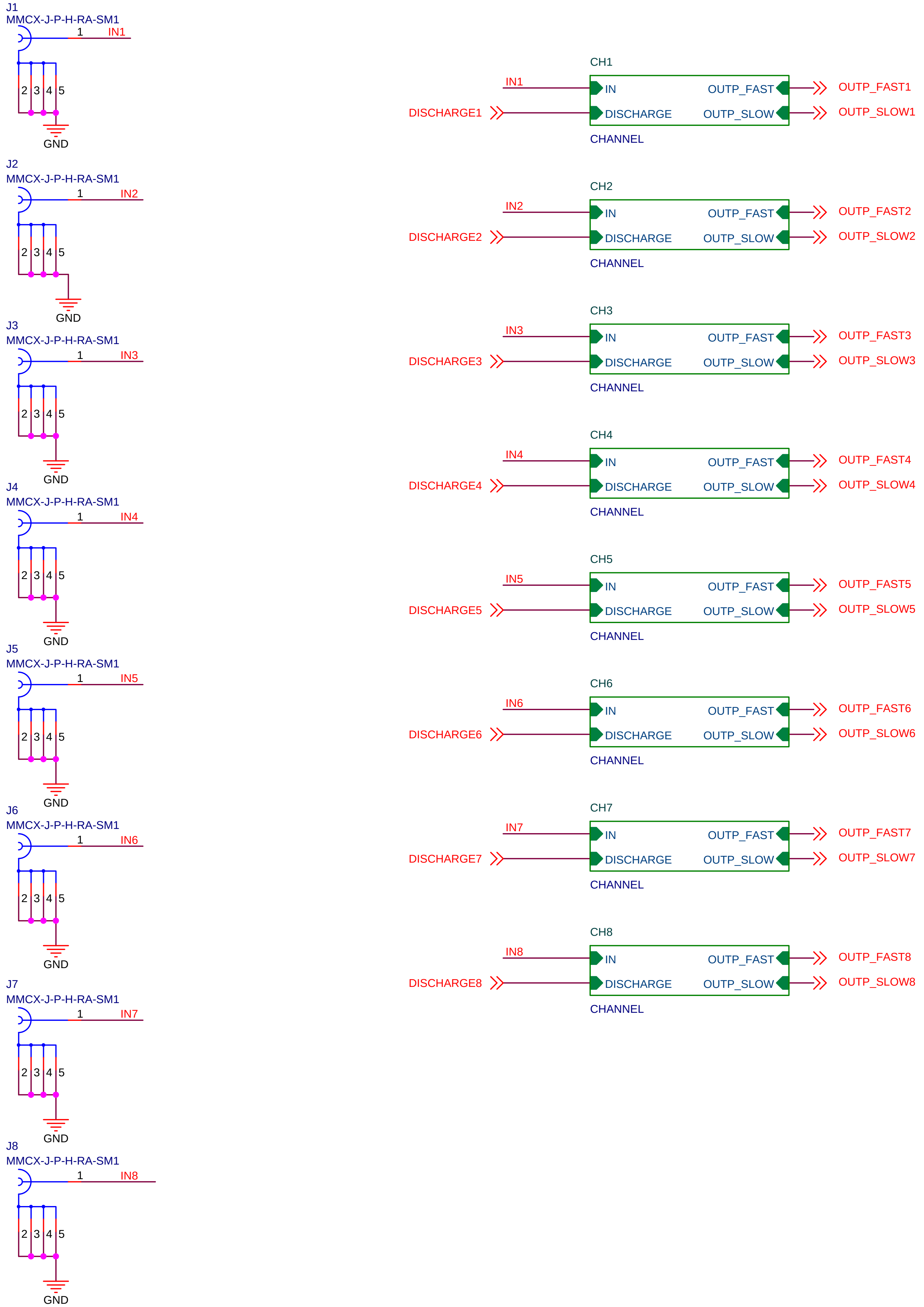
Erstellt am	von	Geprüft am	von	Freigegeben am	von	Revision		
28.09.2006	**M.Kress**	24.10.2006	**S.Baumann**	25.10.2006	**R.Tauras**	00	Seite:	1+

PADIWA-AMPS1

Capture CIS Standard Bill Of Materials - Compressed Report
Report Created on Thursday May 23 14:15:53 2013

Layouter = P.Skott
Designer = M.Traxler

Item Number	Quantity	Part Referenc	DESCRIPTION	PART_CASE	Value	MANUFACTUI	MANUFACTUI	DATASHEET	GSI_STOCK_N	COMMISSION	APPROVED	COMPONENT_ID
1	84	C1,C4,C6-C19,	Capacitor, Cer	SMD-0402	100n					G.May	G.May	24583
2	7	C2,C3,C5,C38,	Capacitor, Cer	SMD-1206	100u	GRM31CR60J:	Murata	K:\GsiLib\Data		M.Traxler	P.Skott	25187
3	20	C20-C26,C53,(	Capacitor, Cer	SMD-0402	68n					G.May	G.May	21811
4	15	C27-C33,C203	Capacitor, Cer	SMD-0402	33n	GRM155R71E	Murata			G.May	G.May	21809
5	16	C34,C35,C208	Capacitor, Cer	SMD-0402	10n	GRM36X7R10	Murata			G.May	G.May	21804
6	32	C253,C256,C2	Capacitor, Cer	SMD-0402	220n	GRM155R61A	Murata	K:\GsiLib\Data		G.May	G.May	21813
7	8	C258,C268,C2	Capacitor, Cer	SMD-0402	2.7p					E.Badura	G.May	21770
8	16	C333-C348	Capacitor, Cer	SMD-0402	1u	GRM155R61A	Murata			G.May	G.May	21815
9	8	C355-C362	Capacitor, Cer	SMD-0402	220p					J.Hoffmann	S.Voltz	20914
10	1	C363	Capacitor, Cer	SMD-0402	4.7u	C1005X5R0J4	TDK	K:\GsiLib\Data		M.Traxler	P.Skott	25745
11	1	D2	Diode, Zener,	DO-214AA	SMBJ5339-TP	SMBJ5339-TP	Micro Comme	K:\GsiLib\Data		M.Traxler	S.Voltz	25682
12	8	D8-D15	Diode, High-S	SOD-882	1N4148WLP	1N4148WLP	Micro Comme	K:\GsiLib\Data		M.Traxler	P.Skott	25739
13	8	DL1-DL8	LED, Single, G	SMD-0402	SML-P11MT	SML-P11MT	Rohm	K:\GsiLib\Data		M.Traxler	P.Skott	25441
14	2	E1,E2	Connector, Dr		3.2mm	Do not order	None			P.Wieczorek	G.May	24737
15	1	F1	Fuse, SMD, Fa	SMD-0402	2A	0402SFF200F/	Tyco	K:\GsiLib\Data		J.Hoffmann	S.Voltz	25103
16	8	J1-J8	Connector, Ja		MMCX-J-P-H-I	MMCX-J-P-H-I	Samtec	K:\GsiLib\Data		M.Traxler	S.Voltz	25681
17	1	J9	Connector, Pi		5-104935-5	5-104935-5	Tyco	K:\GsiLib\Data		M.Traxler	P.Skott	24537
18	1	J10	Connector, Pi		5-826629-0	5-826629-0	AMP	K:\GsiLib\Data		H.Klingbeil	G.May	22988
19	1	J11	Connector, So		ZF5-20-01	ZF5S-20-01-T-	Samtec	K:\GsiLib\Data		J.Hoffmann	S.Voltz	20936
20	1	JOUT1	Connector, Pi		8930E-040-17	8930E-040-17	KEL	K:\GsiLib\Data		M.Traxler	S.Voltz	25633
21	1	JPOW1	Connector, So		37203-1AE0-0	37203-1AE0-0	3M	K:\GsiLib\Data		J.Hoffmann	S.Voltz	25193
22	3	L1,L2,L60	Inductor, RF-C	SMD-1806	BLM41PG471	BLM41PG471	Murata	K:\GsiLib\Data		M.Traxler	S.Voltz	24601
23	33	L3,L5,L8,L10,L	Inductor, RF-C	SMD-0402	BLM15HG102	BLM15HG102	Murata	K:\GsiLib\Data		K.Koch	S.Voltz	24974
24	24	L4,L6,L7,L9,L1	Inductor, Pow		330uH	CBC2518T331	Taiyo Yuden	K:\GsiLib\Data		M.Traxler	P.Skott	25737
25	8	Q1,Q3,Q5,Q7,	Transistor, NP	SOT-323	BFS520	BFS520	NXP	K:\GsiLib\Data		M.Traxler	P.Skott	25738
26	8	Q2,Q4,Q6,Q8,	Transistor, NP	TSFP-4	BFP740FE632	BFP740FE632	Infineon	K:\GsiLib\Data		M.Traxler	P.Skott	25541
27	2	R2,R141	Resistor, Thicl	SMD-0402	4.7k					G.May	G.May	22835
28	8	R4-R9,R12,R1	Resistor, Thicl	SMD-0402	1.47k					G.May	G.May	21169
29	27	R14,R17,R26,I	Resistor, Thicl	SMD-0402	10k	RC1005F103C	Samsung			G.May	G.May	21248
30	1	R15	Resistor, Thicl	SMD-0402	5.6k					G.May	G.May	22837
31	9	R16,R24,R33,I	Resistor, Thicl	SMD-0402	62k					G.May	G.May	22856
32	8	R18,R27,R36,I	Resistor, Thicl	SMD-0402	200k					G.May	G.May	21372
33	24	R19,R28,R37,I	Resistor, Thicl	SMD-0402	220R					G.May	G.May	22809
34	8	R20,R29,R38,I	Resistor, Thicl	SMD-0402	12k					G.May	G.May	22842
35	8	R21,R30,R39,I	Resistor, Thicl	SMD-0402	680R					G.May	G.May	22821
36	8	R22,R31,R40,I	Resistor, Thicl	SMD-0402	300R					G.May	G.May	22812
37	8	R23,R32,R41,I	Resistor, Thicl	SMD-0402	820R					G.May	G.May	22822
38	8	R25,R34,R43,I	Resistor, Thicl	SMD-0402	53.6R					G.May	G.May	21031
39	16	R90,R92,R94,I	Resistor, Thicl	SMD-0402	22k					G.May	G.May	22845
40	1	R143	Resistor, Thicl	SMD-0402	4.3k					G.May	G.May	22834
41	1	TEMP_SENSO	IC-Mixedsigna	uSOP-8	DS18B20U+	DS18B20U+	Maxim	K:\GsiLib\Data		M.Traxler	S.Voltz	24395
42	2	U4,ULDOAMP	IC-Power, Vol	DFN8	LT1965EDD	LT1965EDD	Linear Techno	K:\GsiLib\Data		M.Traxler	P.Skott	25026
43	1	U5	IC-Power, Vol	DFN6	LTC3025-1	LTC3025EDC	Linear Techno	K:\GsiLib\Data		M.Traxler	P.Skott	24929
44	1	UMACH1	IC-Digital, FPG	ftBGA-256	LCMXO2-4000	LCMXO2-4000	Lattice	K:\GsiLib\Data		M.Traxler	S.Voltz	25639



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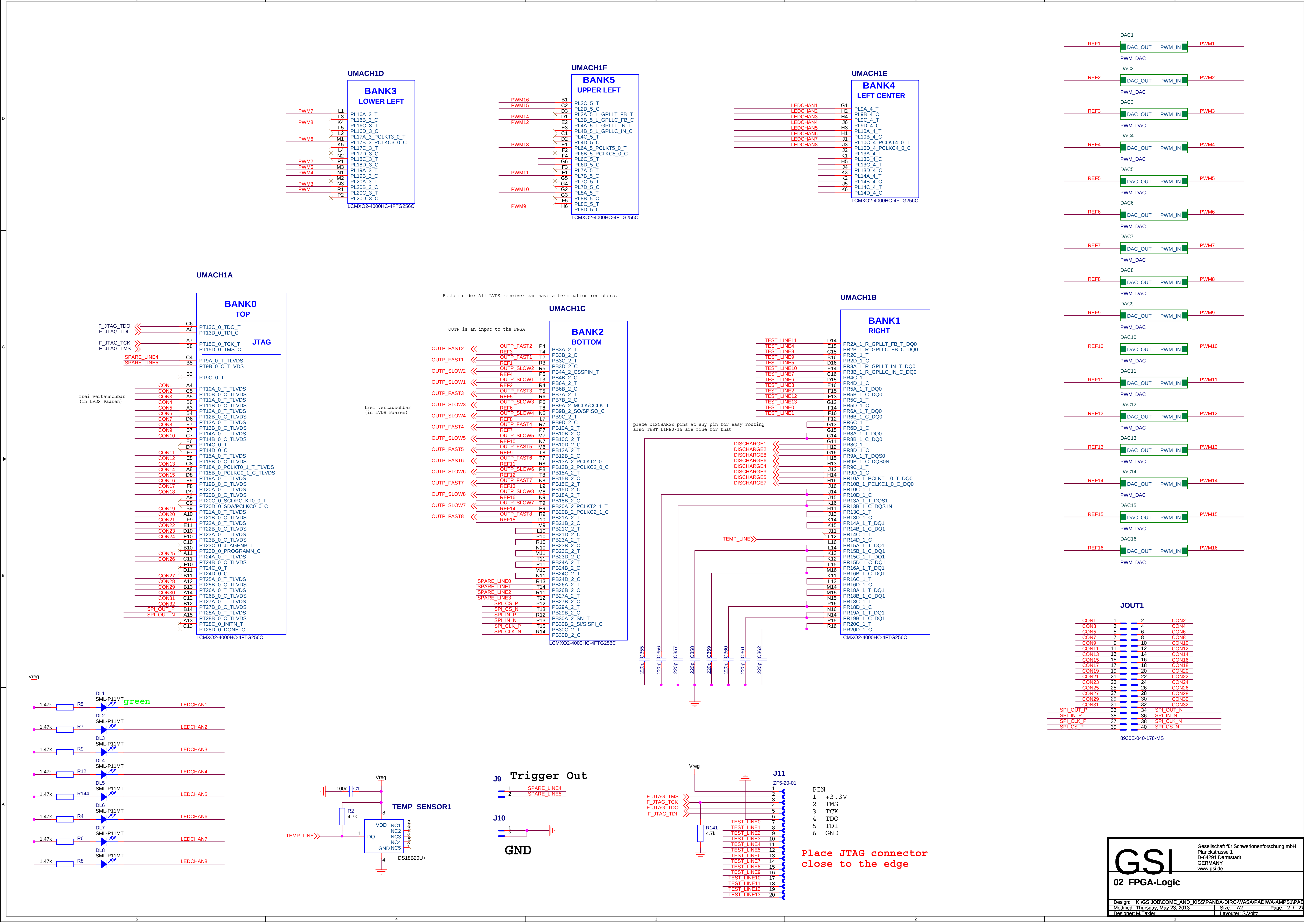
01_ERNI-Connector

Design: K:\GSIJOB\COME_AND_KISS\PANDA-DIRC-WASA\PADIWA-AMPS1\PADI

Modified: Thursday, May 23, 2013 | Size: A3 | Page: 1 / 27

Designer: M.Traxler | Layouter: S.Voltz



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02_FPGA-Logic

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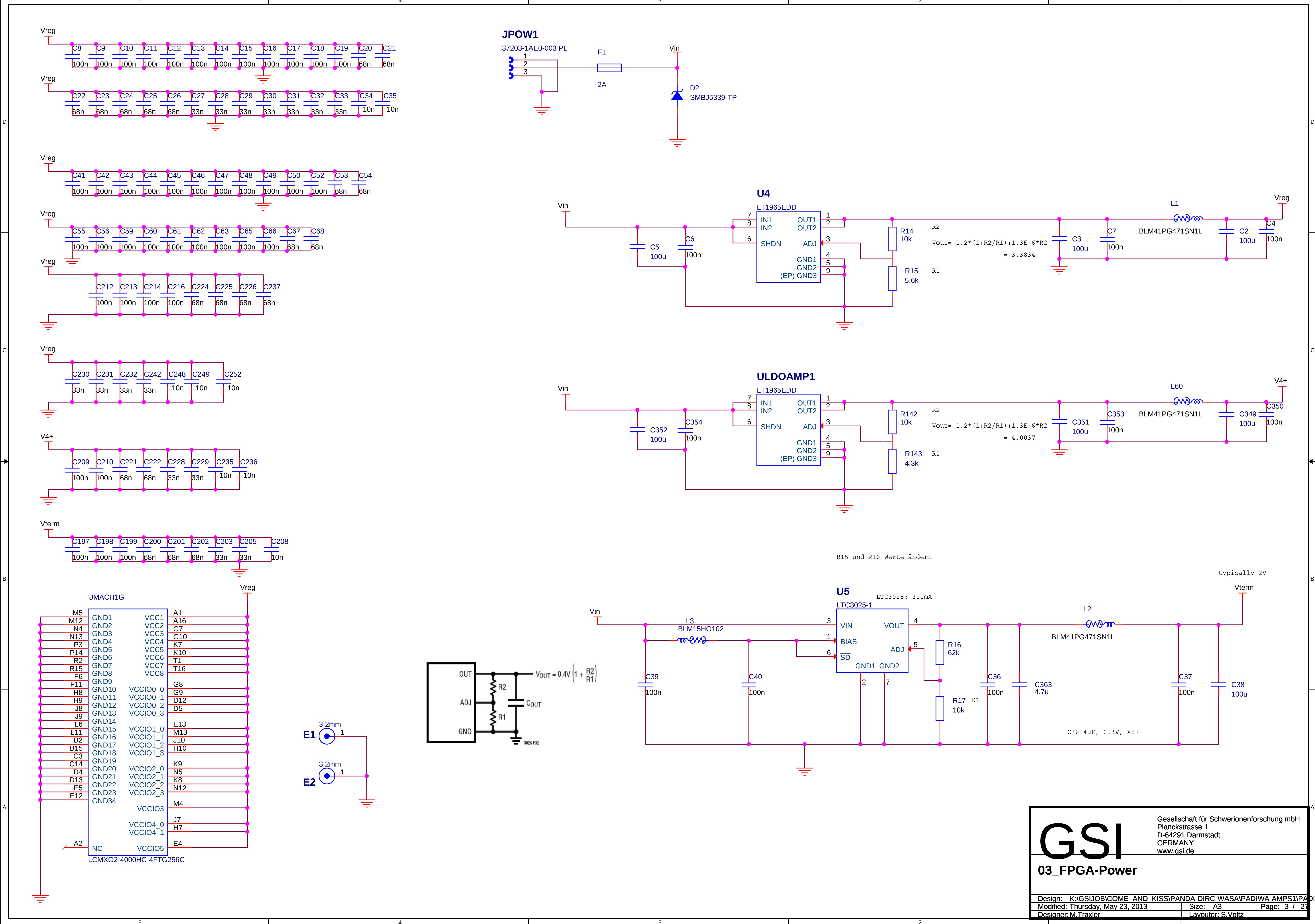
Modified: Thursday, May 23, 2013
Designer: M.Traxler
Size: A2
Page: 2 / 27
Layouter: S.Voltz


JPOW1
37203-1AE0-003 PL
F1
2A
Vin
D2
SMBJ5339-TP
Vreg
Vin
U4
LT1965EDD
IN1
IN2
SHDN
OUT1
OUT2
ADJ
GND1
GND2
(EP) GND3
C5
100u
C6
100n
R14
10k
R15
5.6k
R2
R1
Vout= 1.2*(1+R2/R1)+1.3E-6*R2
= 3.3834
C3
100u
C7
100n
L1
BLM41PG471SN1L
C2
100u
C4
100n
ULDOAMP1
LT1965EDD
C352
100u
C354
100n
R142
10k
R143
4.3k
Vout= 1.2*(1+R2/R1)+1.3E-6*R2
= 4.0037
C351
100u
C353
100n
L60
BLM41PG471SN1L
C349
100u
C350
100n
V4+
R15 und R16 Werte ändern
typically 2V
Vterm
U5
LTC3025: 300mA
LTC3025-1
VIN
BIAS
SD
VOUT
ADJ
GND1 GND2
L3
BLM15HG102
C39
100n
C40
100n
R16
62k
R17
10k
C36
100n
C363
4.7u
L2
BLM41PG471SN1L
C37
100n
C38
100u
C36 4uF, 6.3V, X5R
OUT
ADJ
GND
R2
R1
COUT
VOUT = 0.4V (1 + R2/R1)
UMACH1G
LCMXO2-4000HC-4FTG256C
NC
E1
E2
3.2mm
GSI
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D-64291 Darmstadt
GERMANY
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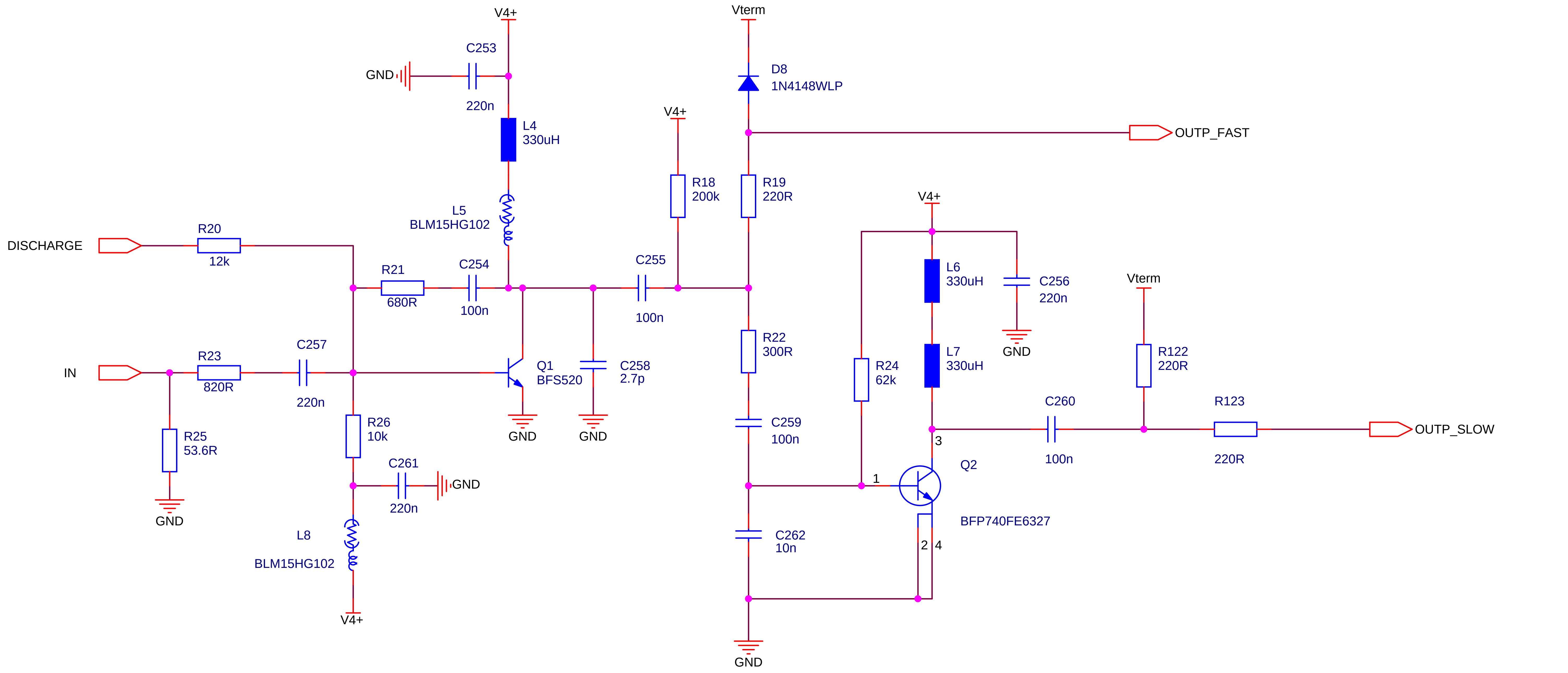
03_FPGA-Power
Design: K:\GSIJOB\COME_AND_KISS\PANDA-DIRC-WASA\PADIWA-AMPS1\PADI
Modified: Thursday, May 23, 2013
Size: A3
Page: 3 / 27
Designer: M.Traxler
Layouter: S.Voltz



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Channel_P

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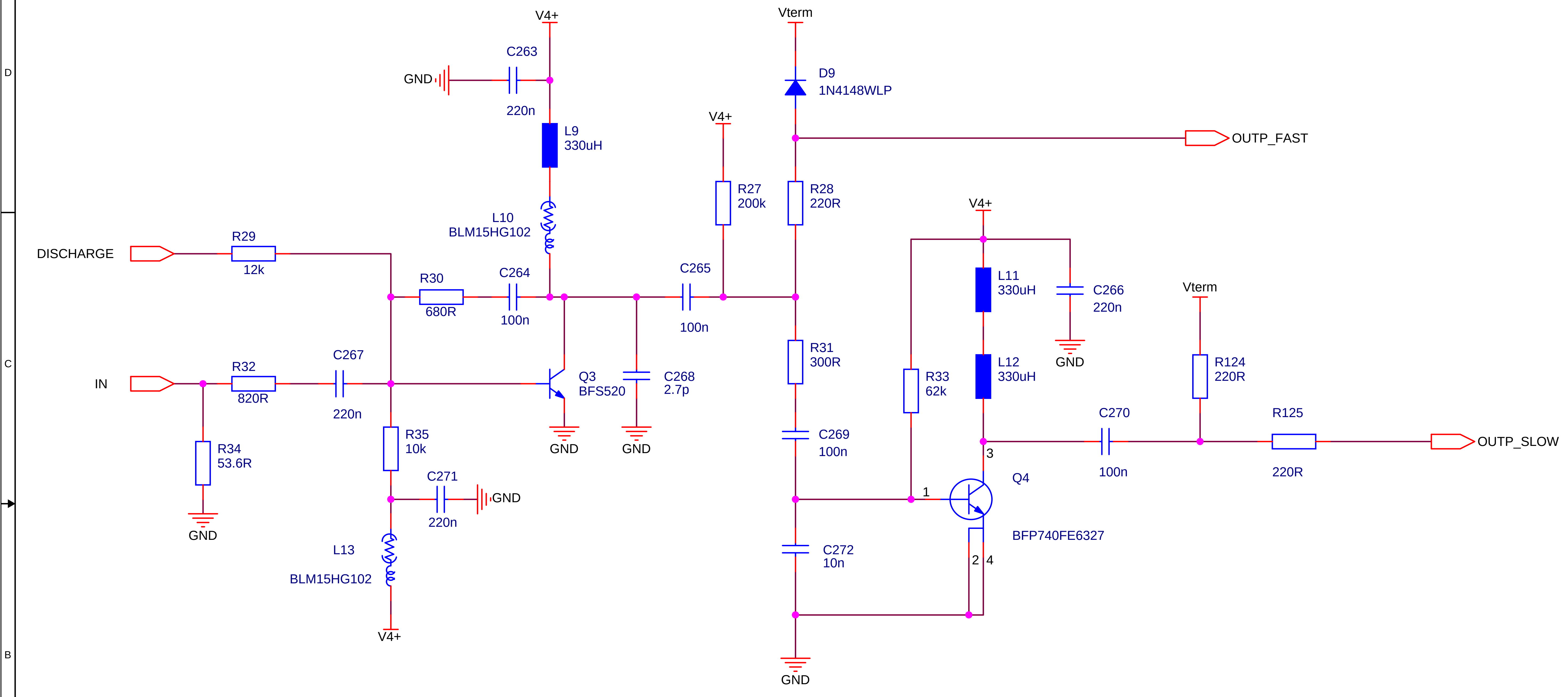
Modified: Thursday, May 23, 2013 | Size: A4 | Page: 4 / 27
Designer: M.Traxler | Layouter: S.Voltz



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Channel_P

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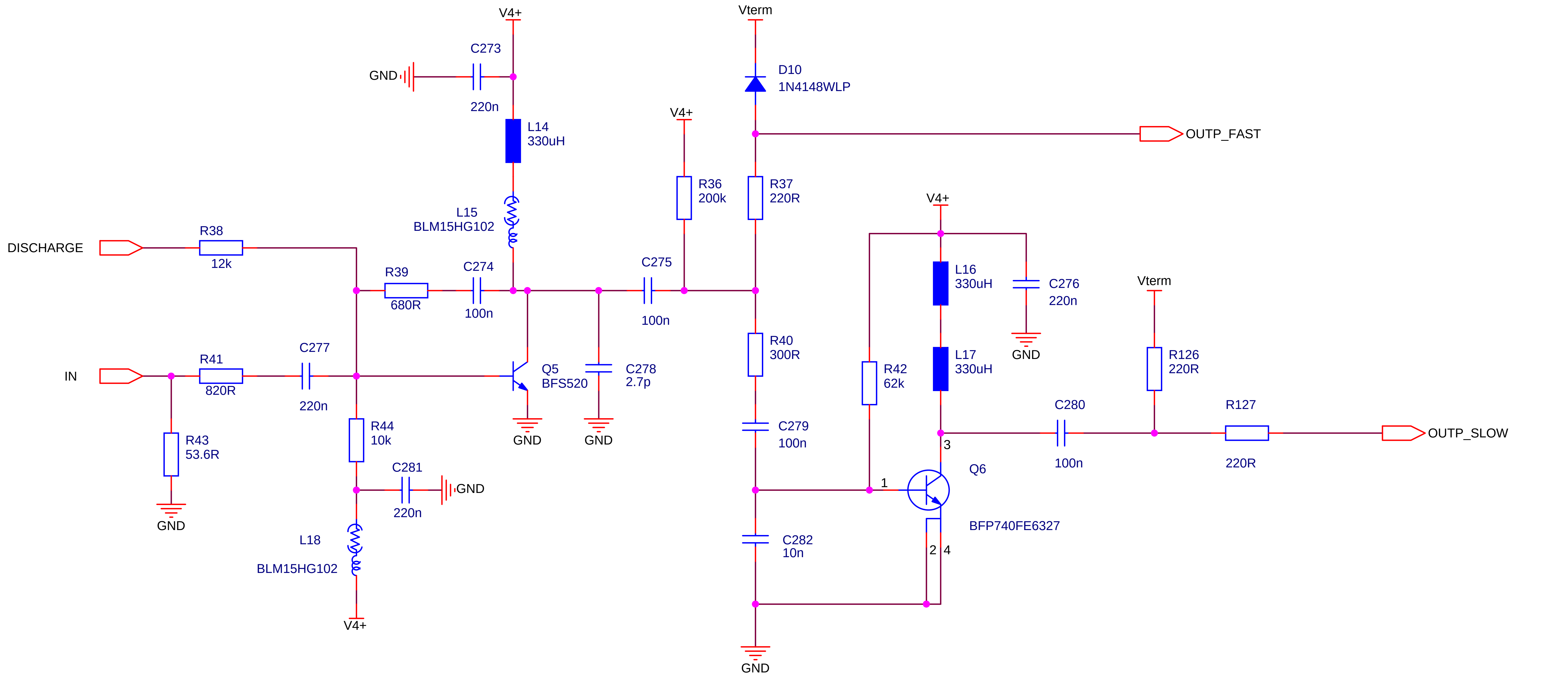
Designer: M.Traxler | Layouter: S.Voltz



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Channel_P

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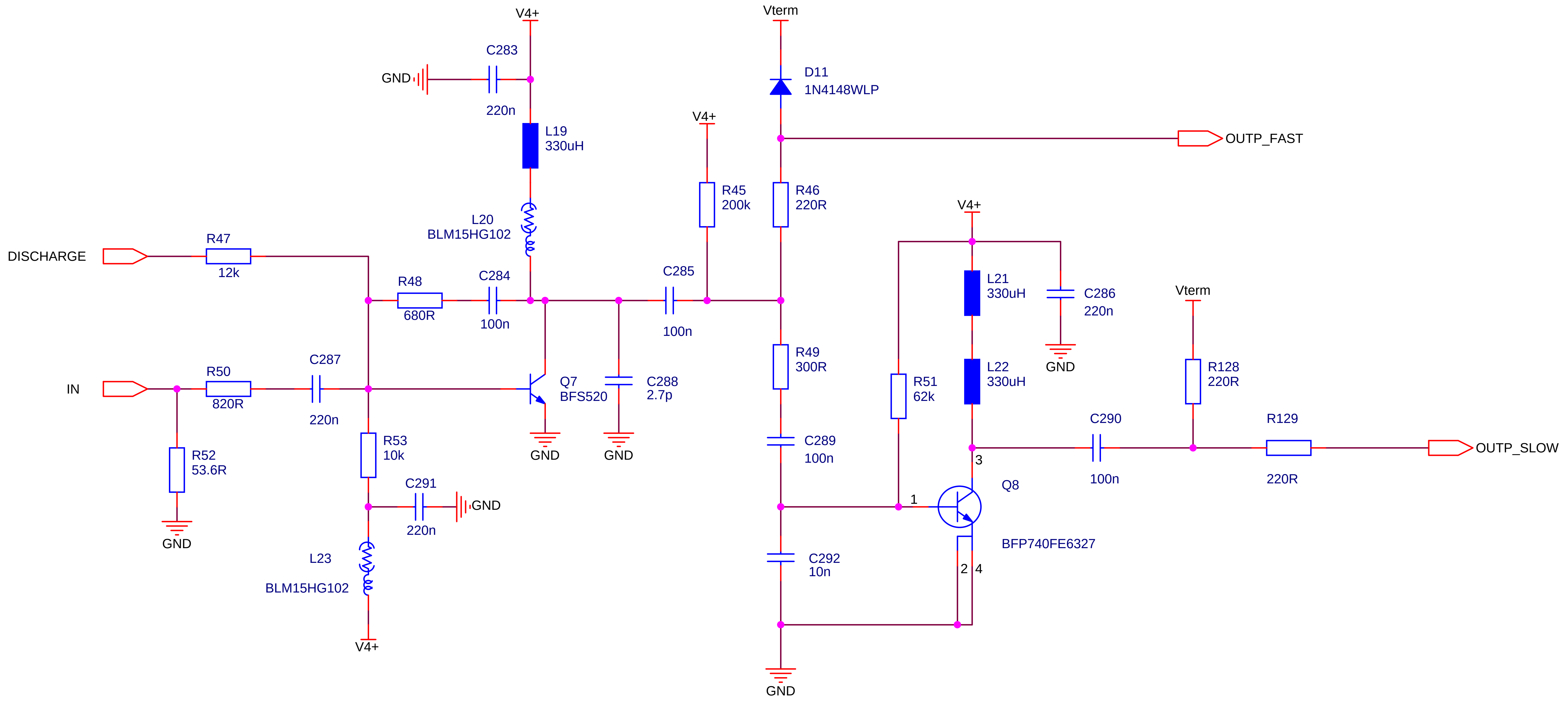
Designer: M.Traxler | Layouter: S.Voltz



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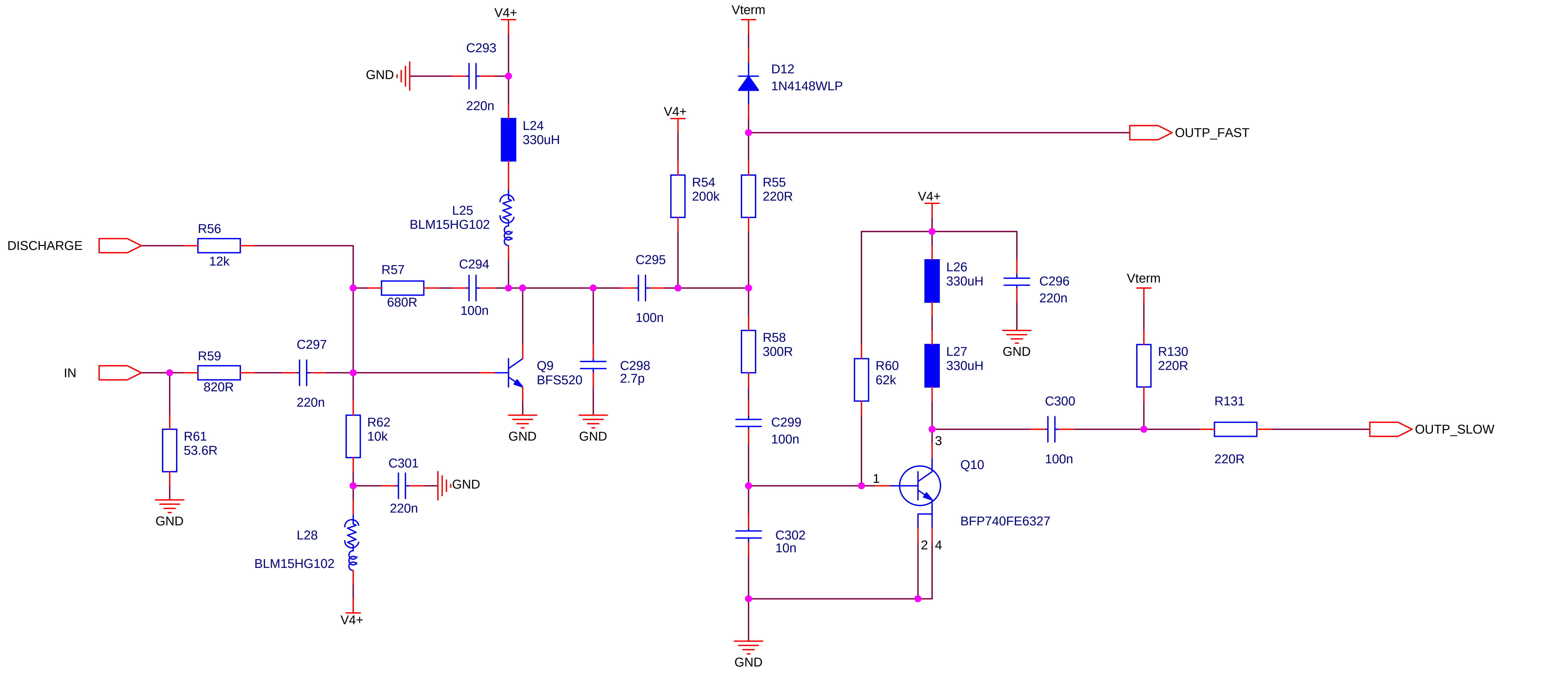
Channel_P

Design: K:\GSIJOB\COME_AND_KISS\PANDA-DIRC-WASA\PADIWA-AMPS1\PADIW
Modified: Thursday, May 23, 2013 | Size: A4 | Page: 7 / 27
Designer: M.Traxler | Layouter: S.Voltz



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Channel_P

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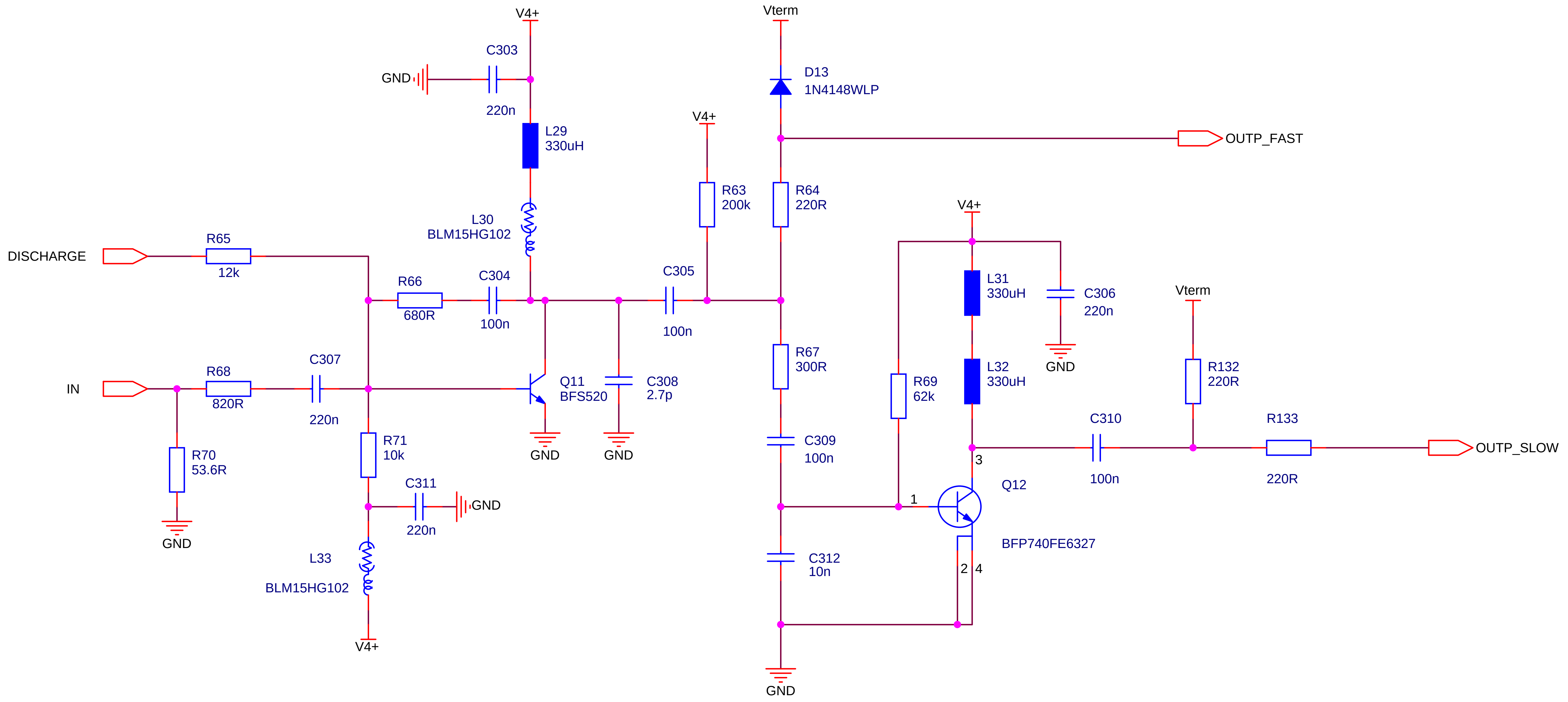
Designer: M.Traxler | Layouter: S.Voltz



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Channel_P

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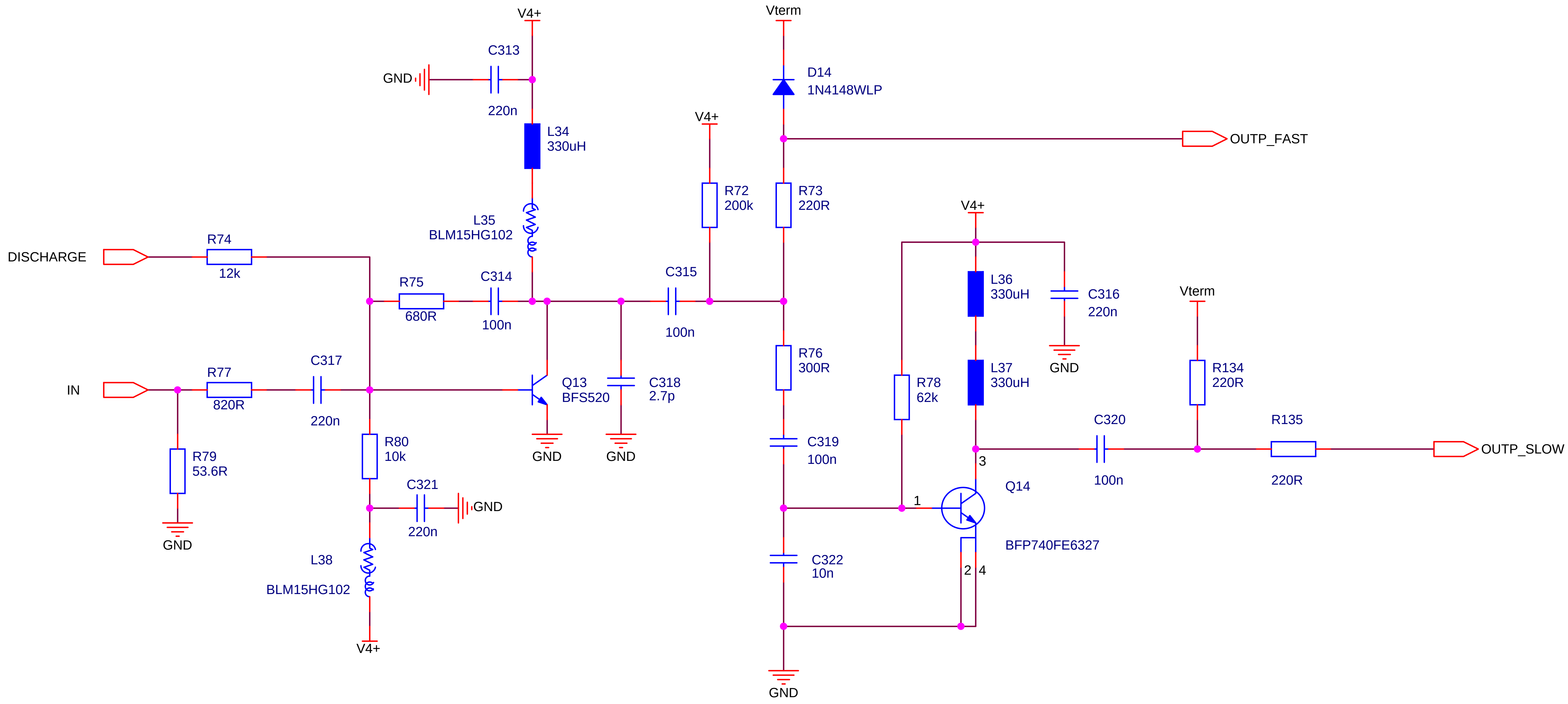
Modified: Thursday, May 23, 2013 | Size: A4 | Page: 9 / 27
Designer: M.Traxler | Layouter: S.Voltz



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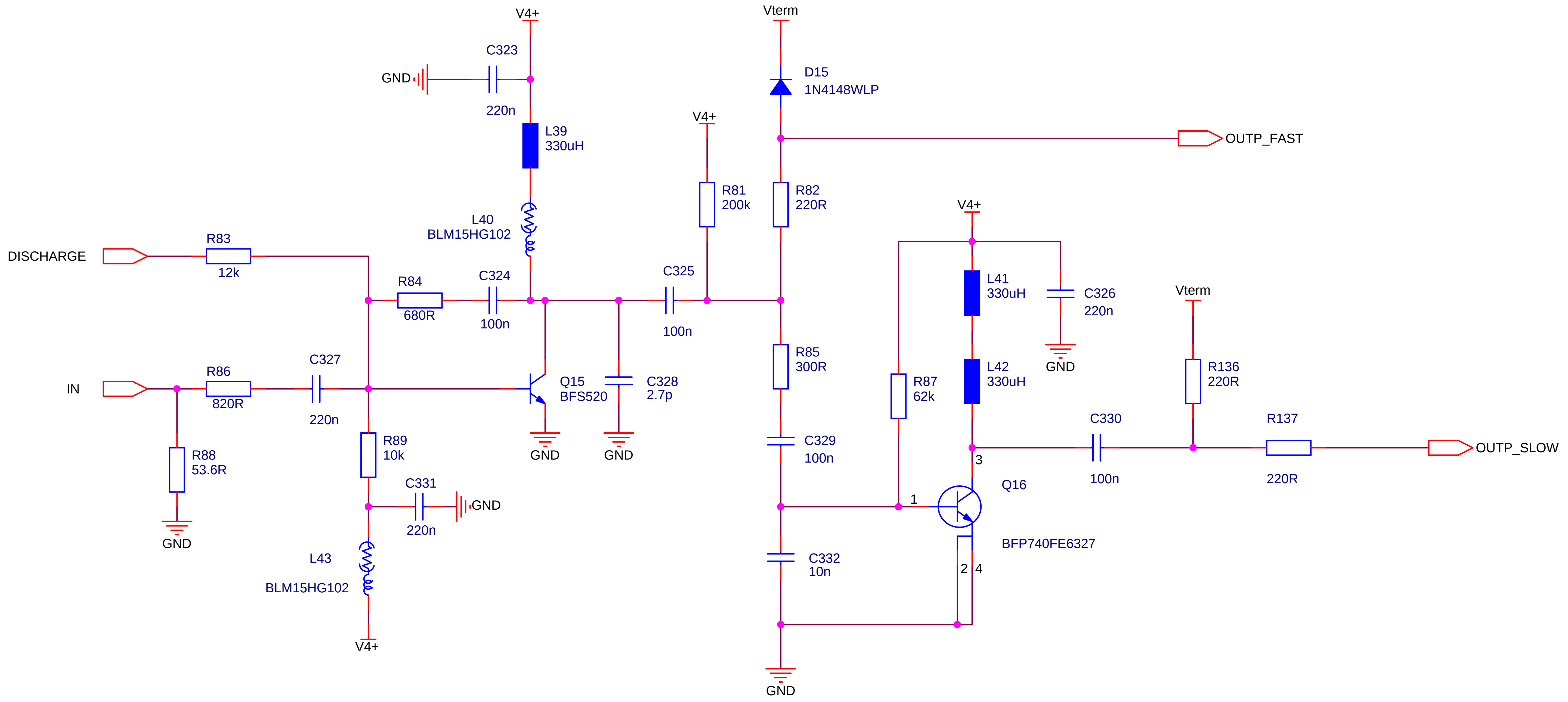
Channel_P

Design: K:\GSIJOB\COME_AND_KISS\PANDA-DIRC-WASA\PADIWA-AMPS1\PADIW
Modified: Thursday, May 23, 2013 | Size: A4 | Page: 10/ 27
Designer: M.Traxler | Layouter: S.Voltz



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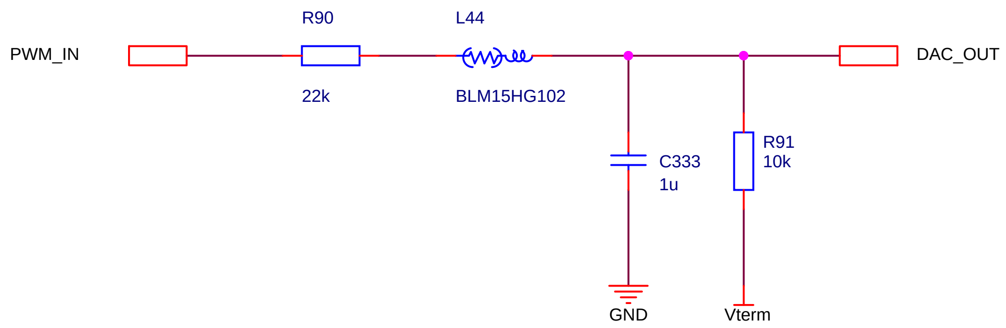
Design: K:\GSIJOB\COME_AND_KISS\PANDA-DIRC-WASA\PADIWA-AMPS1\PADIW
Modified: Thursday, May 23, 2013 | Size: A4 | Page: 11/ 27
Designer: M.Traxler | Layouter: S.Voltz

wire around FPGA, from output side to input side

FPGA-THR

THR-OUT



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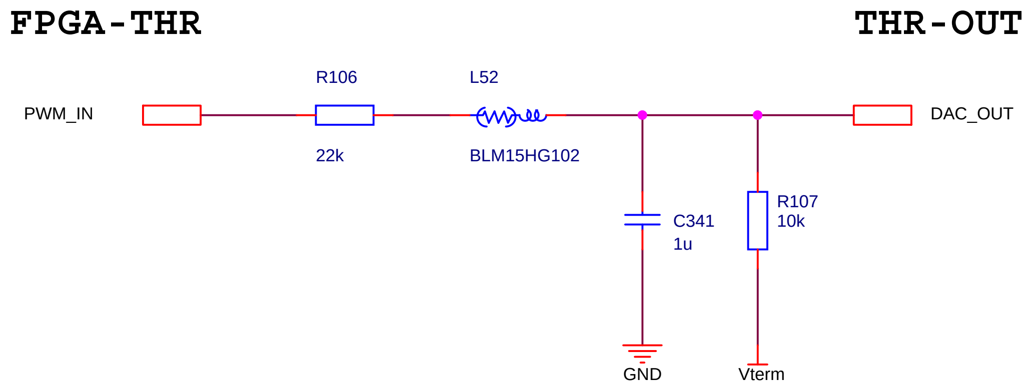
Design: K:\GSIJOB\COME_AND_KISS\PANDA-DIRC-WASA\PADIWA-AMPS1\PADI
Modified: Thursday, May 23, 2013 Size: A3 Page: 12/ 27
Designer: M.Traxler Layouter: S.Voltz

wire around FPGA, from output side to input side



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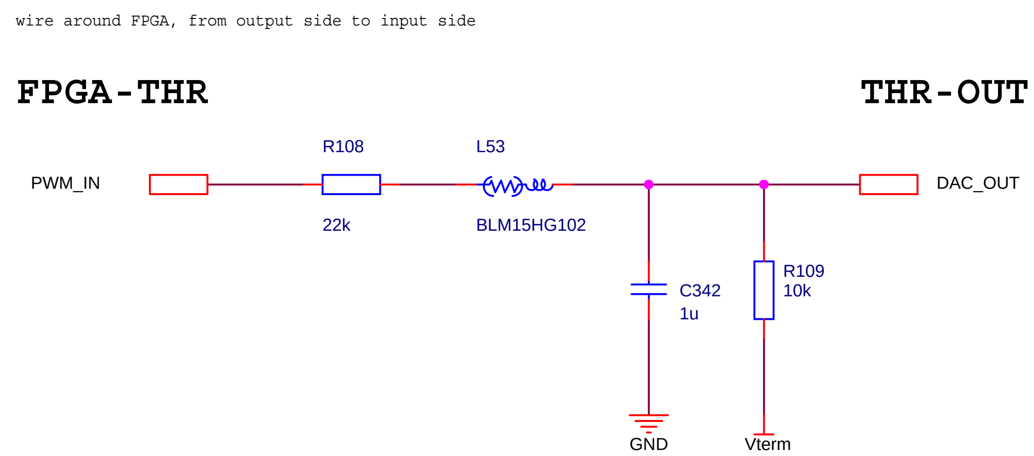
Modified: Thursday, May 23, 2013 | Size: A3 | Page: 13/ 27
Designer: M.Traxler | Layouter: S.Voltz



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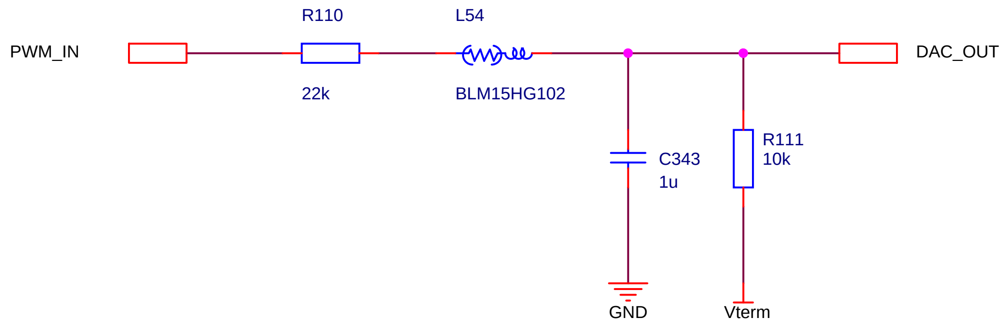
Modified: Thursday, May 23, 2013 | Size: A3 | Page: 14/ 27
Designer: M.Traxler | Layouter: S.Voltz

wire around FPGA, from output side to input side

FPGA-THR **THR-OUT**



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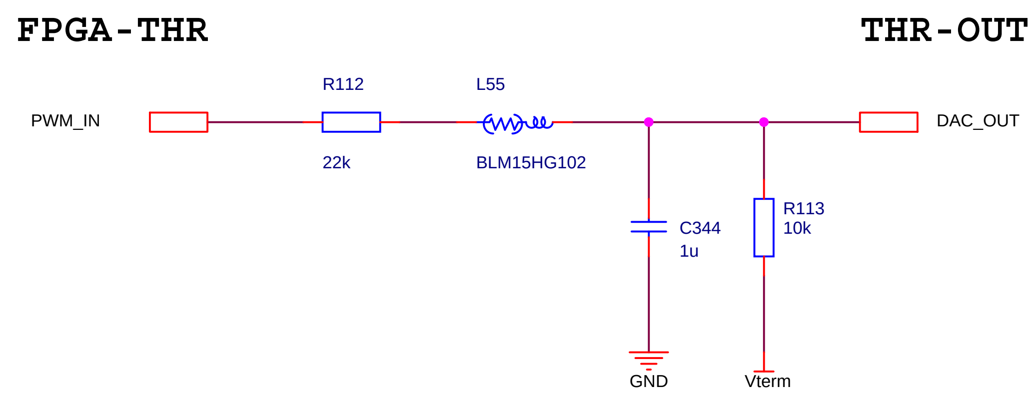
Modified: Thursday, May 23, 2013	Size: A3	Page: 15/ 27
Designer: M.Traxler	Layouter: S.Voltz	

wire around FPGA, from output side to input side



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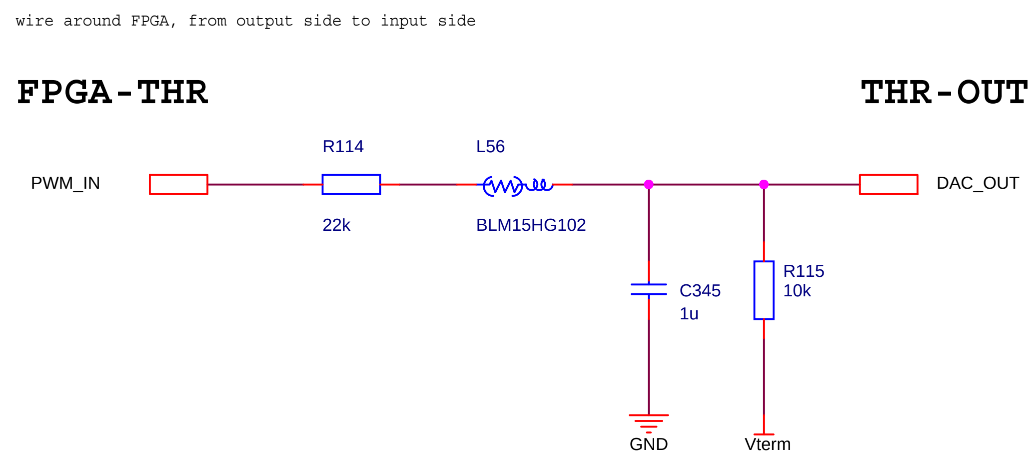
Modified: Thursday, May 23, 2013 | Size: A3 | Page: 16/ 27
Designer: M.Traxler | Layouter: S.Voltz



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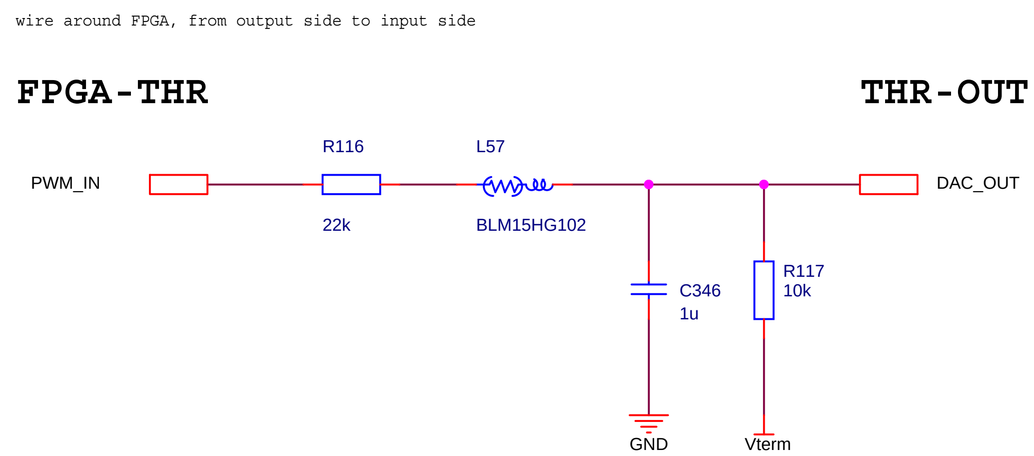
Modified: Thursday, May 23, 2013	Size: A3	Page: 17/ 27
Designer: M.Traxler	Layouter: S.Voltz	



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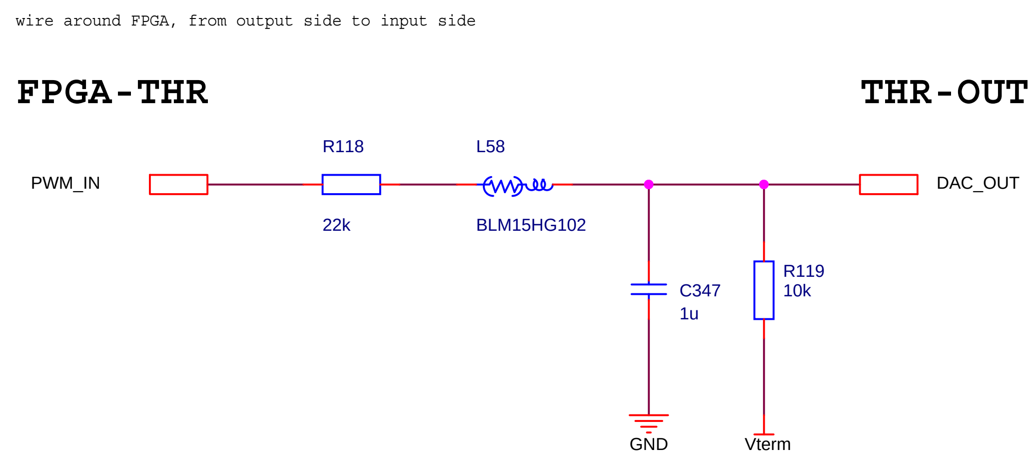
Modified: Thursday, May 23, 2013 | Size: A3 | Page: 18/ 27

Designer: M.Traxler | Layouter: S.Voltz



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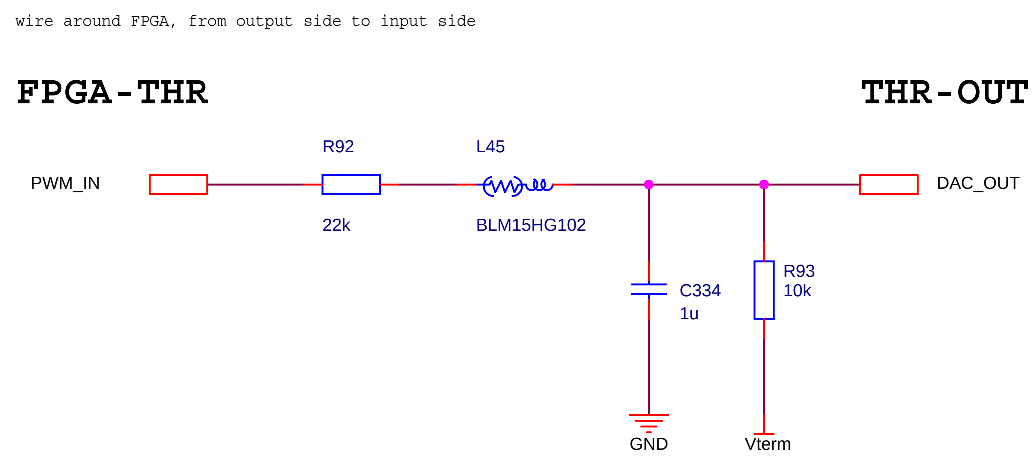
Modified: Thursday, May 23, 2013 Size: A3 Page: 19/ 27
Designer: M.Traxler Layouter: S.Voltz



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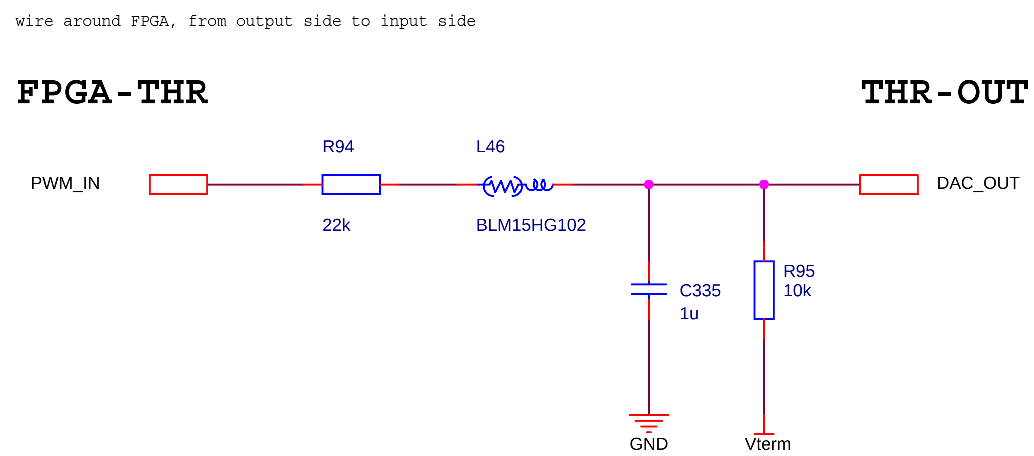
Modified: Thursday, May 23, 2013	Size: A3 Page: 20/ 27
Designer: M.Traxler	Layouter: S.Voltz



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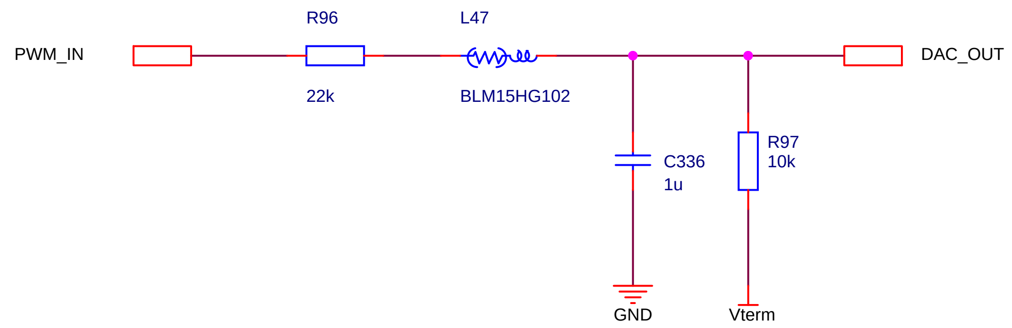
Modified: Thursday, May 23, 2013 | Size: A3 | Page: 21/ 27

Designer: M.Traxler | Layouter: S.Voltz

wire around FPGA, from output side to input side

FPGA-THR

THR-OUT



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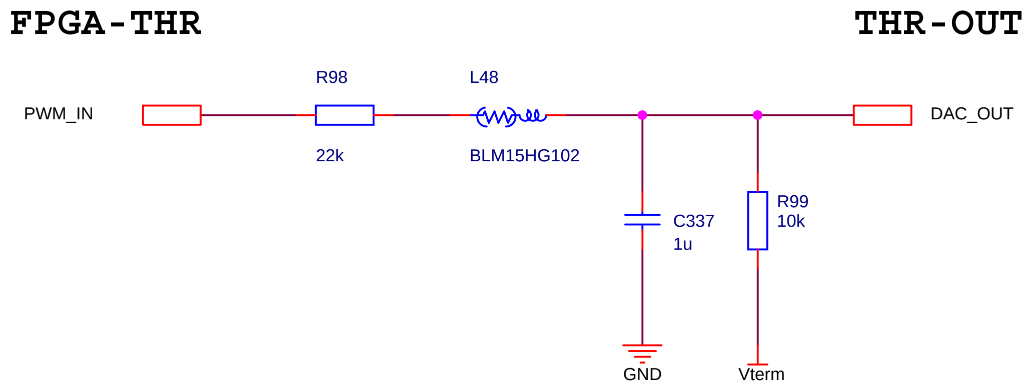
Modified: Thursday, May 23, 2013 | Size: A3 | Page: 22/ 27
Designer: M.Traxler | Layouter: S.Voltz

wire around FPGA, from output side to input side



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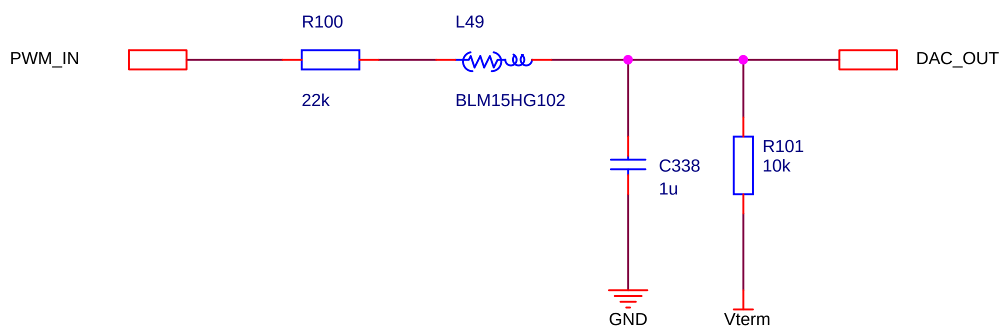
Modified: Thursday, May 23, 2013	Size: A3 Page: 23/ 27
Designer: M.Traxler	Layouter: S.Voltz

wire around FPGA, from output side to input side

FPGA-THR **THR-OUT**



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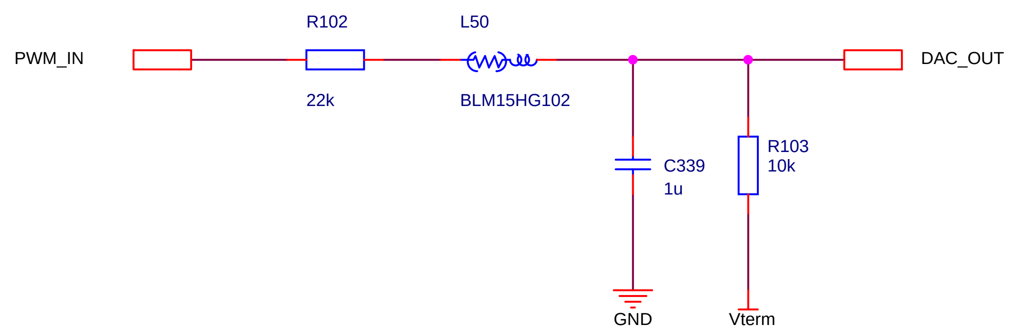
Modified: Thursday, May 23, 2013	Size: A3	Page: 24/ 27
Designer: M.Traxler	Layouter: S.Voltz	

wire around FPGA, from output side to input side

FPGA-THR **THR-OUT**



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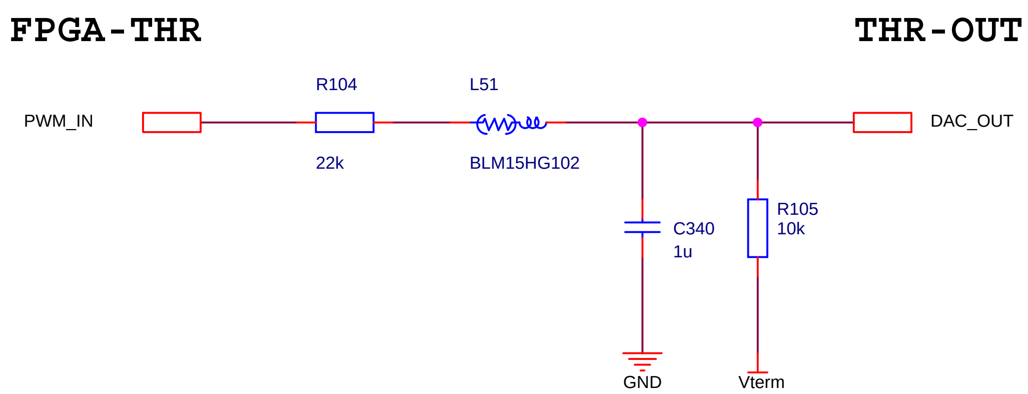
Modified: Thursday, May 23, 2013	Size: A3	Page: 25/ 27
Designer: M.Traxler	Layouter: S.Voltz	

wire around FPGA, from output side to input side



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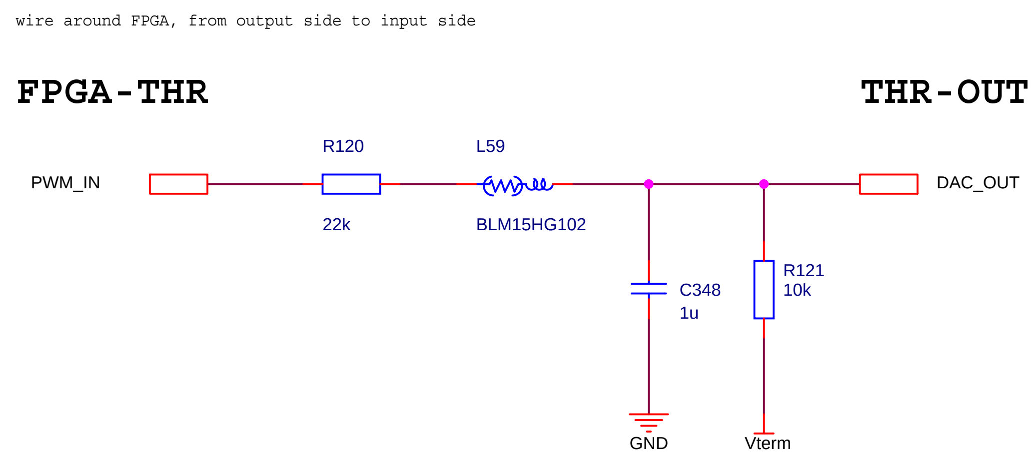
Modified: Thursday, May 23, 2013	Size: A3 Page: 26/ 27
Designer: M.Traxler	Layouter: S.Voltz



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