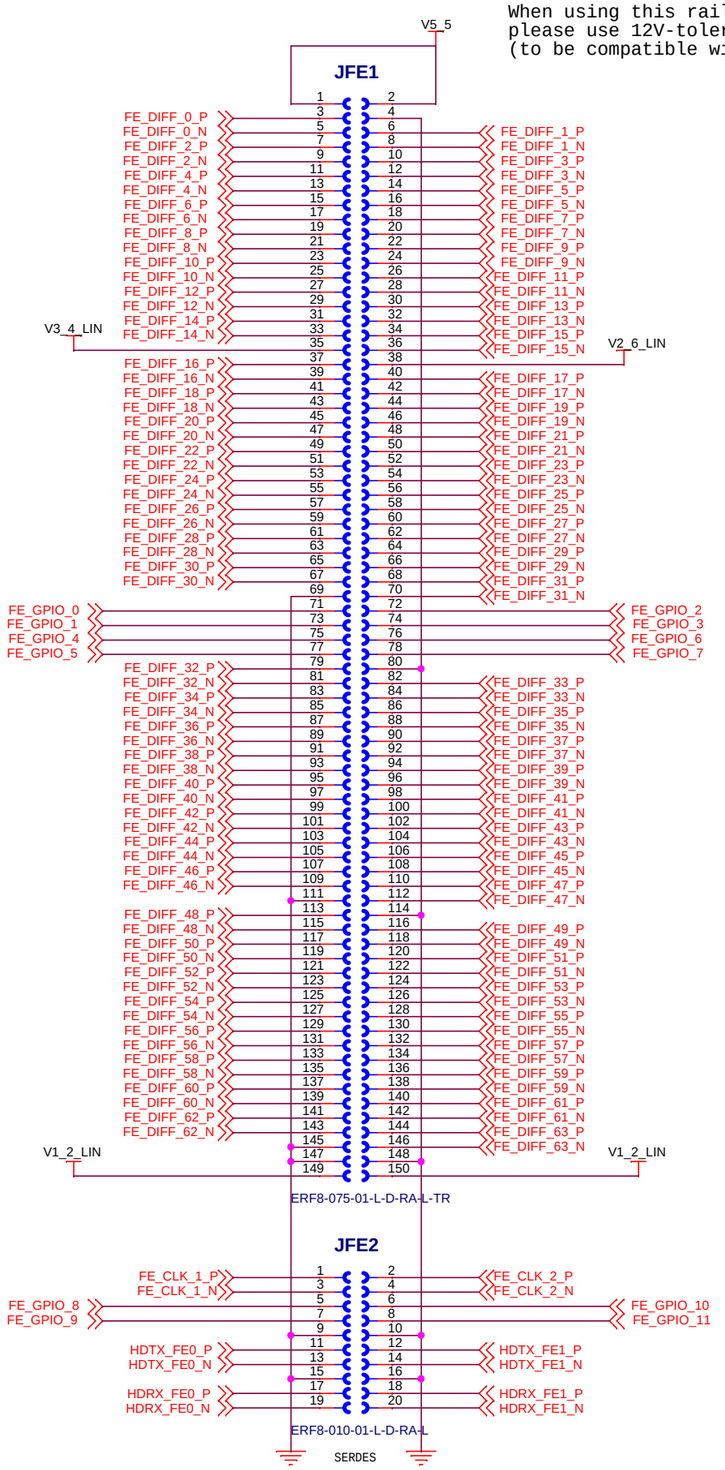
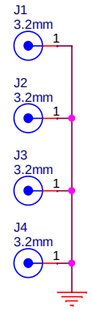
When using this rail (V5_5) on a front-end,
please use 12V-tolerant converters if possible!
(to be compatible with TAMEX4 module)





Bohrungen in den Ecken der Leiterplatte platzieren

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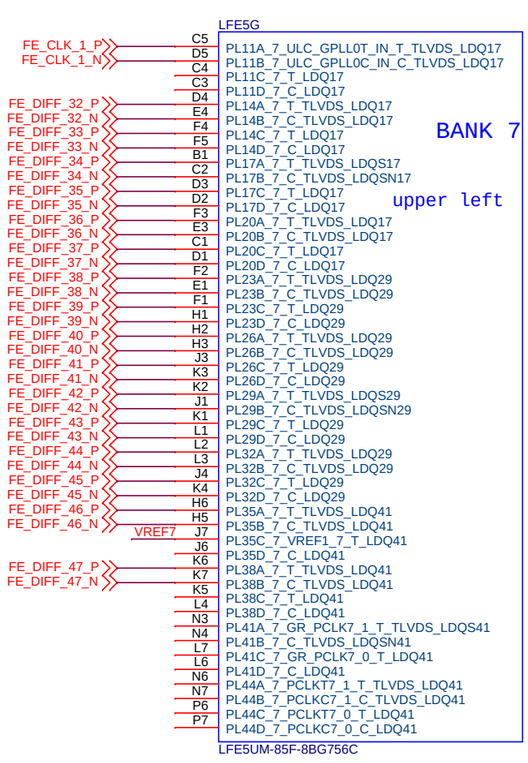
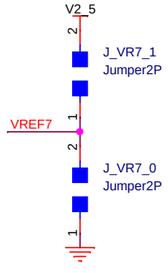
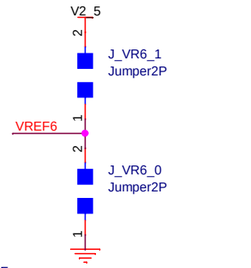
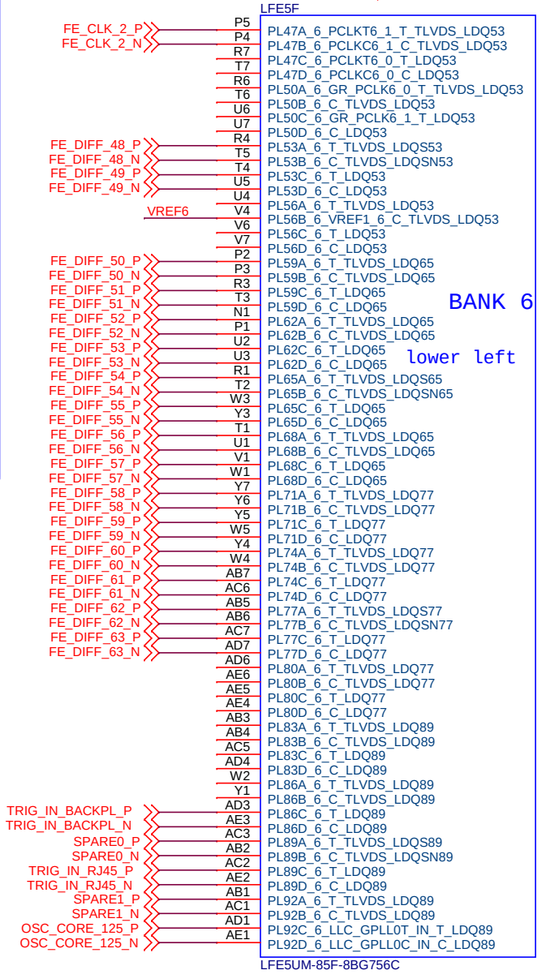
TRB5SC1 - FRONT IO

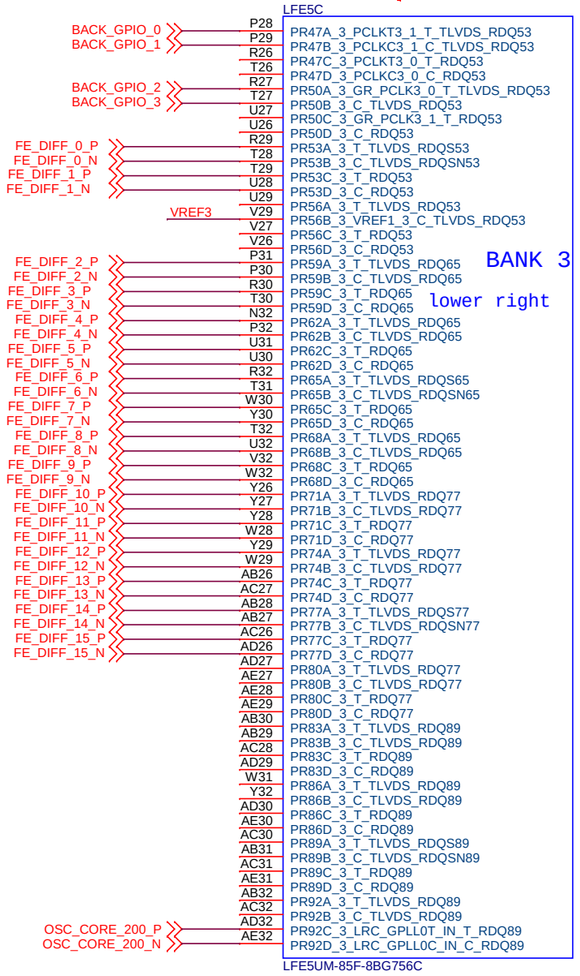
Design: K:\GSIJOB\HADES\TRB5SC\TRB5SC2\TRB5SC2.DSN	
Modified: Monday, March 02, 2020	Size: A3 Page: 1 / 7
Designer: H. Heggen	Layouter: H.Kavan

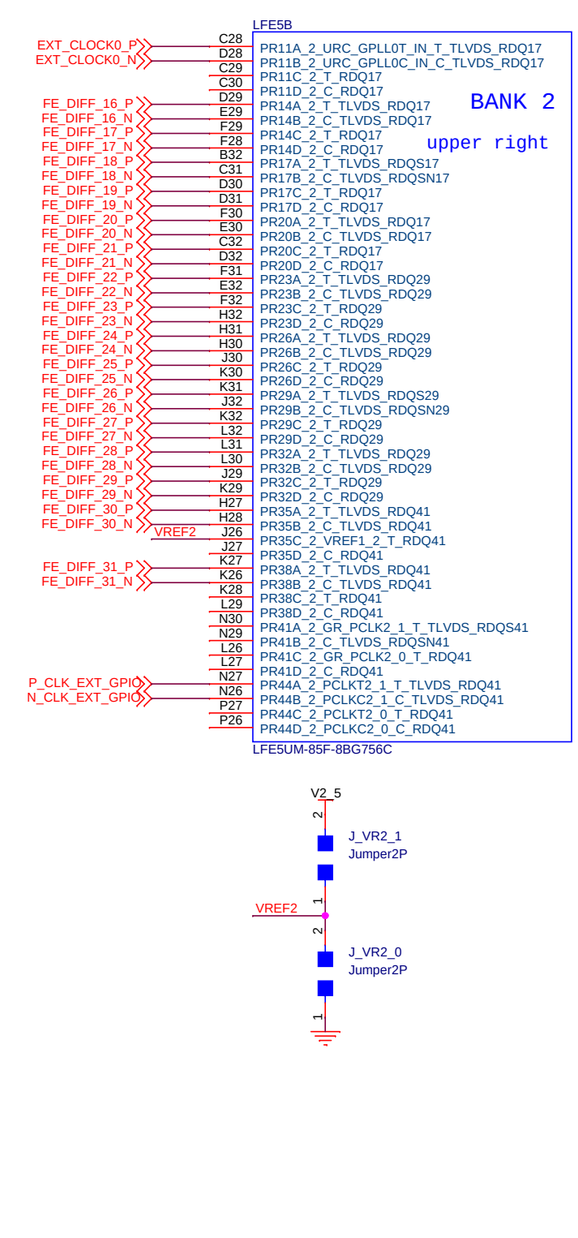


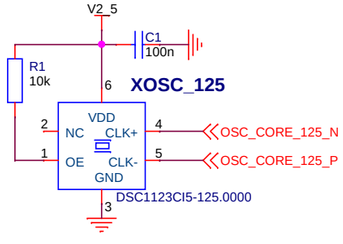


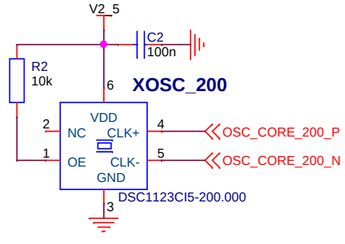












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TRB5SC1 - LVDS Banks

Design: K:\GSIJOB\HADES\TRB5SC\TRB5SC2\TRB5SC2.DSN
Modified: Monday, March 02, 2020
Designer: H. Heggen
Size: A3
Page: 2 / 7
Layouter: H.Kavan

LFE5K

B3 PT4A_0_ULC_GPLL1T_IN_T
B4 PT4B_0_ULC_GPLL1C_IN_C
A2 PT6A_0_T
A3 PT6B_0_C
A4 PT9A_0_T
A5 PT9B_0_C
D7 PT11A_0_T
C7 PT11B_0_C
B7 PT13A_0_T
A7 PT13B_0_C
F8 PT15A_0_T
E8 PT15B_0_C
D8 PT18A_0_T
C8 PT18B_0_C
B8 PT20A_0_T
A8 PT20B_0_C
F9 PT22A_0_T
D9 PT22B_0_C
C9 PT24A_0_T
A9 PT24B_0_C
F10 PT27A_0_T
E10 PT27B_0_C
D10 PT29A_0_T
C10 PT29B_0_C
B10 PT31A_0_T
A10 PT31B_0_C
F11 PT33A_0_T
E11 PT33B_0_C
D11 PT36A_0_T
C11 PT36B_0_C
B11 PT38A_0_T
A11 PT38B_0_C
F13 PT40A_0_T
D13 PT40B_0_C
C13 PT42A_0_T
A13 PT42B_0_C
F14 PT45A_0_T
E14 PT45B_0_C
D14 PT47A_0_T
C14 PT47B_0_C
B14 PT49A_0_T
A14 PT49B_0_C
F15 PT51A_0_T
D15 PT51B_0_C
C15 PT54A_0_T
A15 PT54B_0_C
F16 PT56A_0_T
E16 PT56B_0_C
D16 PT58A_0_T
C16 PT58B_0_C
B16 PT60A_0_GR_PCLK0_1_T
A16 PT60B_0_GR_PCLK0_0_C
B17 PT63A_0_PCLKT0_1_T
C17 PT63B_0_PCLKC0_1_C
D17 PT65A_0_PCLKT0_0_T
PT65B_0_PCLKC0_0_C

BANK 0
2.5V

TMP_ALERT
I2C_SCL
I2C_SDA
IN_SELECT_EXT_CLOCK

LFE5UM-85F-8BG756C

LFE5A

E17 PT69A_1_PCLKT1_1_T
F17 PT69B_1_PCLKC1_1_C
A18 PT71A_1_PCLKT1_0_T
C18 PT71B_1_PCLKC1_0_C
D18 PT74A_1_GR_PCLK1_0_T
F18 PT74B_1_GR_PCLK1_1_C
A19 PT76A_1_T
B19 PT76B_1_C
C19 PT78A_1_T
D19 PT78B_1_C
E19 PT80A_1_T
F19 PT80B_1_C
A20 PT83A_1_T
C20 PT83B_1_C
D20 PT85A_1_T
F20 PT85B_1_C
A22 PT87A_1_T
B22 PT87B_1_C
C22 PT89A_1_T
D22 PT89B_1_C
E22 PT92A_1_T
F22 PT92B_1_C
A23 PT94A_1_T
B23 PT94B_1_C
C23 PT96A_1_T
D23 PT96B_1_C
E23 PT98A_1_T
F23 PT98B_1_C
A24 PT101A_1_T
C24 PT101B_1_C
D24 PT103A_1_T
F24 PT103B_1_C
A25 PT105A_1_T
B25 PT105B_1_C
C25 PT107A_1_T
D25 PT107B_1_C
E25 PT110A_1_T
F25 PT110B_1_C
A26 PT112A_1_T
B26 PT112B_1_C
C26 PT114A_1_T
D26 PT114B_1_C
A28 PT116A_1_T
A29 PT116B_1_C
A30 PT119A_1_T
A31 PT119B_1_C
B29 PT121A_1_URC_GPLL1T_IN_T
B30 PT121B_1_URC_GPLL1C_IN_C

FE_GPIO_0
FE_GPIO_1
FE_GPIO_2
FE_GPIO_3
FE_GPIO_4
FE_GPIO_5
FE_GPIO_6
FE_GPIO_7
FE_GPIO_8
FE_GPIO_9
FE_GPIO_10
FE_GPIO_11
HDR_IO_23
HDR_IO_1
HDR_IO_6
HDR_IO_2
HDR_IO_20
HDR_IO_19
HDR_IO_22
HDR_IO_0
HDR_IO_4
HDR_IO_8
HDR_IO_17
HDR_IO_18
HDR_IO_16
HDR_IO_3
HDR_IO_9
HDR_IO_7
HDR_IO_15
HDR_IO_5
HDR_IO_12
HDR_IO_13
HDR_IO_10
HDR_IO_14
HDR_IO_21
LED1
LED2
HDR_IO_11
LED3
LED4
LED5
LED6
LED7
LED8

BANK1
2.5V

LFE5UM-85F-8BG756C

LFE5D

AM28 PB96A_4_T
AM29 PB96B_4_C
AL28 PB98A_4_T
AK28 PB98B_4_C
AK32 PB101A_4_T
AJ32 PB101B_4_C
AM30 PB103A_4_T
AL30 PB103B_4_C
AK31 PB105A_4_T
AJ31 PB105B_4_C
AM31 PB107A_4_T
AL32 PB107B_4_C
AG28 PB110A_4_T
AG29 PB110B_4_C
AJ28 PB112A_4_T
AH28 PB112B_4_C
AH30 PB114A_4_T
AG30 PB114B_4_C
AK29 PB116A_4_T
AK30 PB116B_4_C
AH32 PB119A_4_T
AG32 PB119B_4_C
AJ29 PB121A_4_T
AJ30 PB121B_4_C

LED_CLOCK_GREEN
LED_CLOCK_RED
LED_TRIGGER_GREEN
LED_TRIGGER_RED
ENPIRION_CLOCK
SFP1_MOD0
SFP1_MOD1
SFP1_MOD2
SFP1_TX_DIS
SFP1_TX_FAULT
SFP1_RATE_SEL
SFP1_LOS
SFP1_LED_GREEN
SFP1_LED_RED
SFP1_LED_YELLOW
LED_EXT_CLOCK

BANK 4
3.3V

LFE5UM-85F-8BG756C

JGPIO1

HDR_IO_0	1	2	HDR_IO_1
HDR_IO_2	3	4	HDR_IO_3
HDR_IO_4	5	6	HDR_IO_5
HDR_IO_6	7	8	HDR_IO_7
HDR_IO_8	9	10	HDR_IO_9
HDR_IO_10	11	12	HDR_IO_11
HDR_IO_12	13	14	HDR_IO_13
HDR_IO_14	15	16	HDR_IO_15
HDR_IO_16	17	18	HDR_IO_17
HDR_IO_18	19	20	HDR_IO_19
HDR_IO_20	21	22	HDR_IO_21
HDR_IO_22	23	24	HDR_IO_23
P_CLK_EXT_GPIO	25	26	N_CLK_EXT_GPIO
EN_DCDC	27	28	
	29	30	
V3_3	31	32	V5_5
V2_5	33	34	
	35	36	
JTAG_TMS	37	38	JTAG_TCK
JTAG_TDI	39	40	JTAG_TDO

2540-6002

Steckerbelegung so gut wie möglich mit Text auf dem Board markieren

Place LED close to FPGA

V2_5 C4 100n
U1
DONE1
V2_5 680R R15 SML-P11MT
SN74LVC1G57YZPR
DONE

RST1
KMR223GCT-ND
0R R4
10k R5
V2_5
FPGA_REPROGRAM
RST_OR1
SN74LVC1G57YZPR
0R R6
PROGRAMN

V3_3
R9 DNP
R10 0R
R11 DNP
R12 10k
R13 10k
R14 10k
C3 100n
R16 0R
R17 DNP
R18 0R

LFE5I

FLASH_SCLK AM3
CFG0 AM4
CFG1 AL4
CFG2 AK4
DONE AJ4
INITN AG4
PROGRAMN AH4
JTAG_TCK AK5
JTAG_TDI AJ5
JTAG_TDO AG5
JTAG_TMS AM5

CCLK_8_MCLK/SCK
CFG_0_8
CFG_1_8
CFG_2_8
DONE_8
INITN_8
PROGRAMN_8
TCK_40
TDI_40
TDO_40
TMS_40

BANK 8
CFG[0..2]: 010 (MSB first)
3.3V

V3_3 R84 10k
FPGA_REPROGRAM

AG1 PB4A_8_D7/IO7_T
AH1 PB4B_8_D6/IO6_C
AJ1 PB6A_8_D5/MISO2/IO5_T
AK1 PB6B_8_D4/MOSI2/IO4_C
AL1 PB9A_8_D3/IO3_T
AM2 PB9B_8_D2/IO2_C
AJ2 PB11A_8_D1/MISO/IO1_T
AK2 PB11B_8_D0/MOSI/IO0_C
AG3 PB13A_8_SN/CSN_T
AH3 PB13B_8_CS1N_C
AJ3 PB15A_8_HOLDN/DI/BUSY/CSSPIN/CEN_T
AK3 PB15B_8_DOUT/CSON_C
AL3 PB18A_8_WRITEN

LFE5UM-85F-8BG756C

V2_5
R7 2k
R8 2k
I2C_SCL
I2C_SDA
UUID1
SCL VCC
SDA VSS
24AA02UID
address: 1010XXX
V2_5 C5 100n

UTMP1
I2C_SCL B2
I2C_SDA C2
TMP_ALERT C1
SCL A0
SDA V+
ALERT GND
B1 A1 A2
TMP108
address: 1001000

V2_5
D1 green LED1 680R R19 SML-P11MT
D2 orange LED2 1.8k R20 SML-P11DT
D3 red LED3 1.8k R21 SML-P11UT
D4 yellow LED4 1.8k R23 SML-P11YT
D5 green LED5 680R R29 SML-P11MT
D6 orange LED6 1.8k R30 SML-P11DT
D7 red LED7 1.8k R32 SML-P11UT
D8 yellow LED8 1.8k R34 SML-P11YT

V5_5
R22 4.7k
C7 100n
R24 4.7k
V1_2_LIN
C8 100n
V3_4_LIN
C10 100n
V2_6_LIN
R31 4.7k
C11 100n
R35 4.7k

V3_3
C6 100n
UADC1
VDD 8
GND 3
AIN0 4
AIN1 5
AIN2 6
AIN3 7
SCLK 1 ADC_SCLK
CS 2 ADC_NCS
DOUT 9 ADC_MISO
DIN 10 ADC_MOSI
ADS1018IRUGT

V3_3
R87 4.7k JTAG_TMS
R88 4.7k JTAG_TCK
R89 4.7k JTAG_TDI

Place Flash close to FPGA

V3_3
R25 10k
R26 10k
R27 10k
R28 10k
R33 10k
R85 DNP
FLASH_MOSI
FLASH_SCLK
FLASH_NCS
FLASH_WP
FLASH_HOLD
FLASH1
SI
SCLK
CS
WP
HOLD
Vcc
SO
GND
MX25L6406EZNI-12G
FLASH_MISO
V3_3 C9 100n

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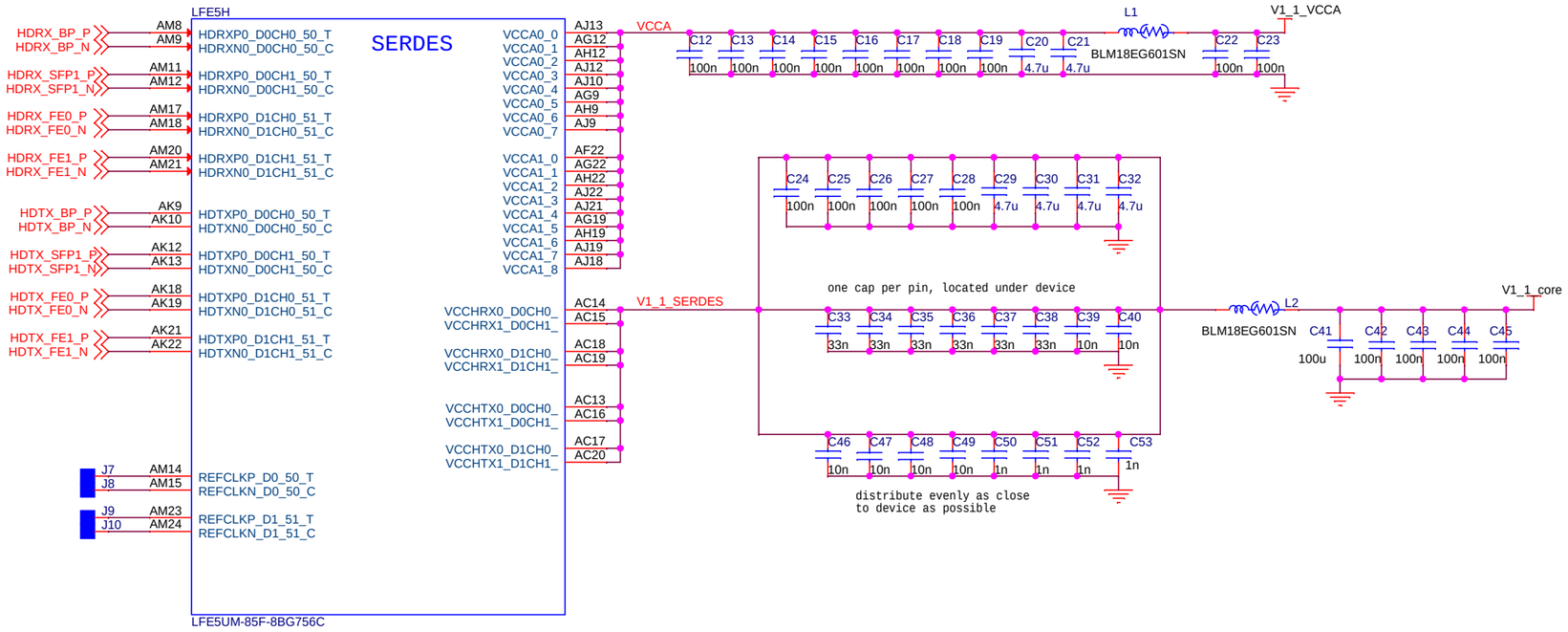
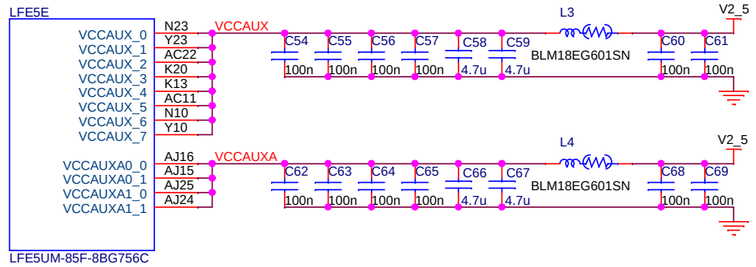
TRB5SC1 - GPIO

Design: K:\GSIJOB\HADES\TRB5SC\TRB5SC2\TRB5SC2.DSN
Modified: Monday, March 02, 2020 Size: A3 Page: 3 / 7
Designer: H. Heggen Layouter: H.Kavan





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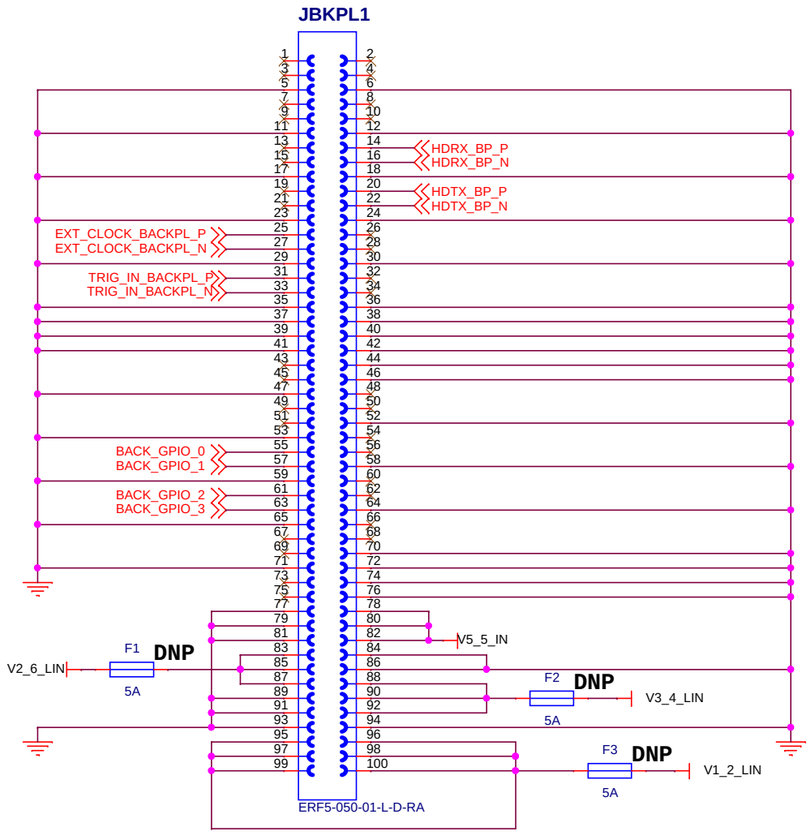
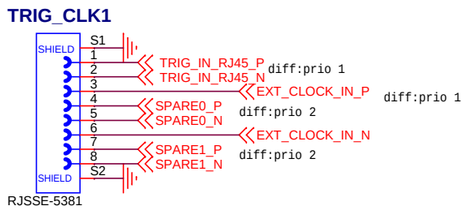
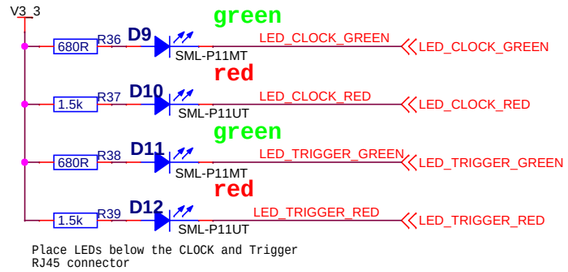
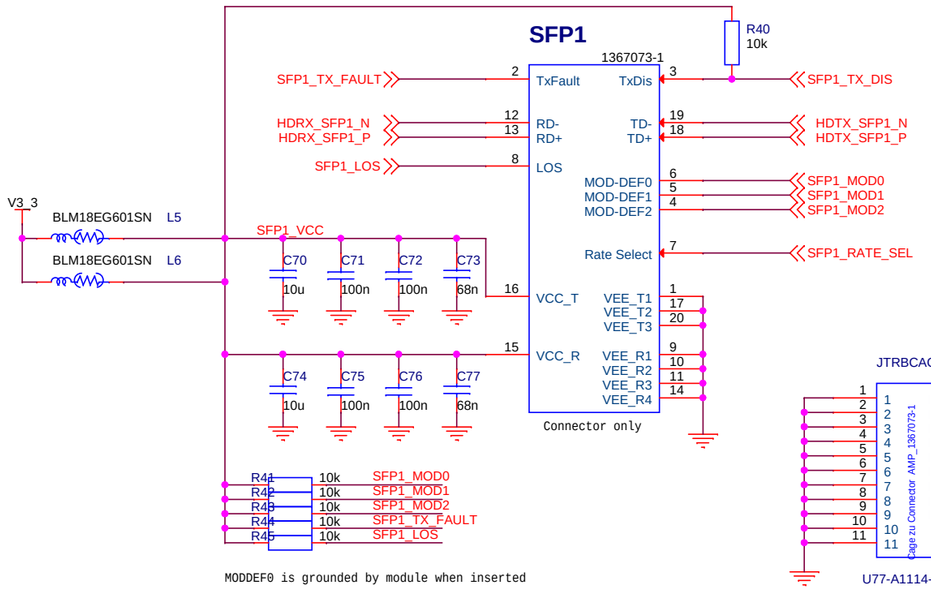
TRB5SC1 - SERDES

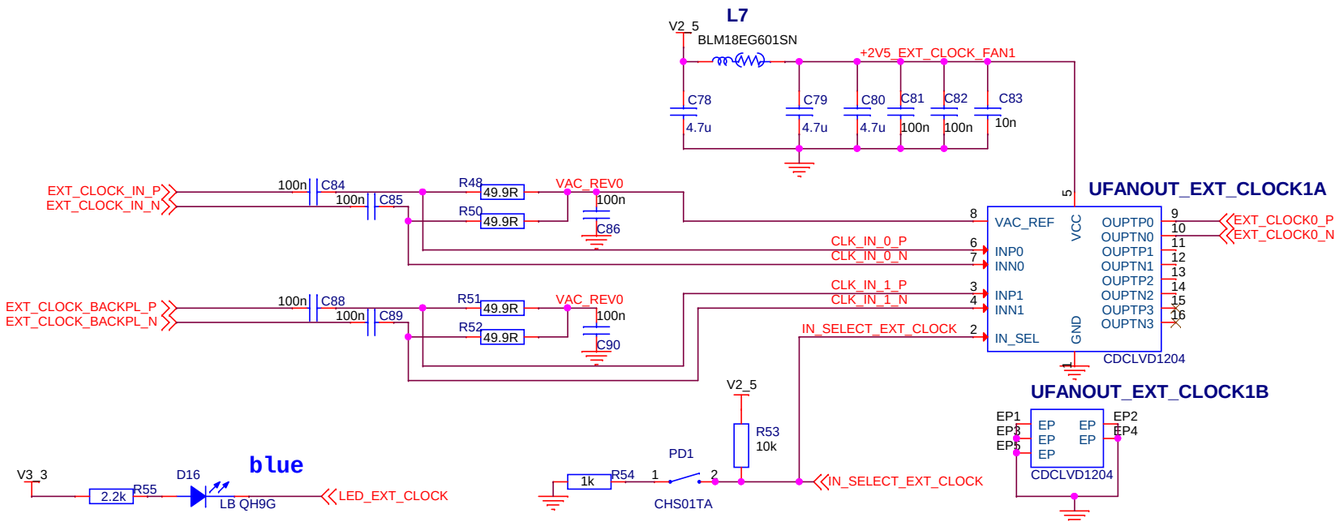
Design: K:\GSIJOB\HADES\TRB5SC\TRB5SC2\TRB5SC2.DSN	
Modified: Monday, March 02, 2020	Size: A3 Page: 4 / 7
Designer: H. Heggen	Layouter: H.Kavan

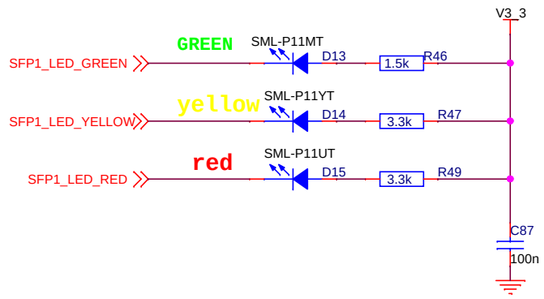












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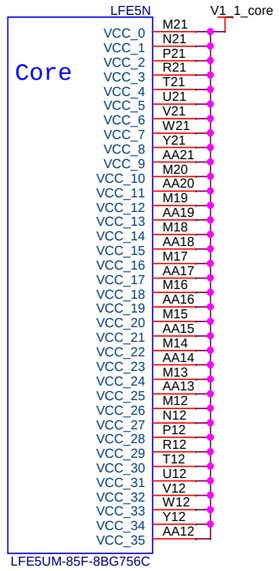
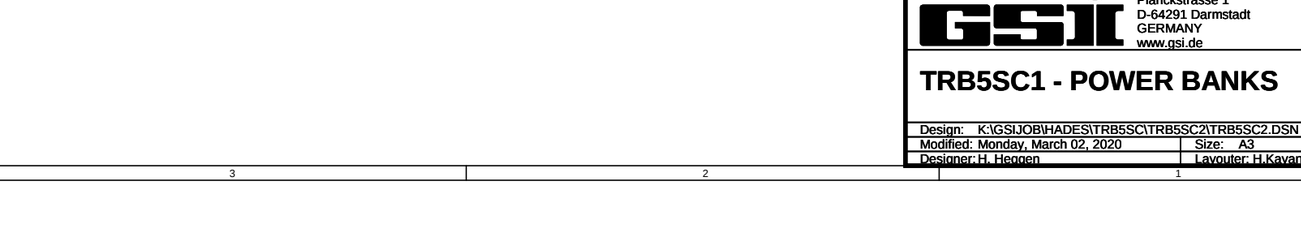
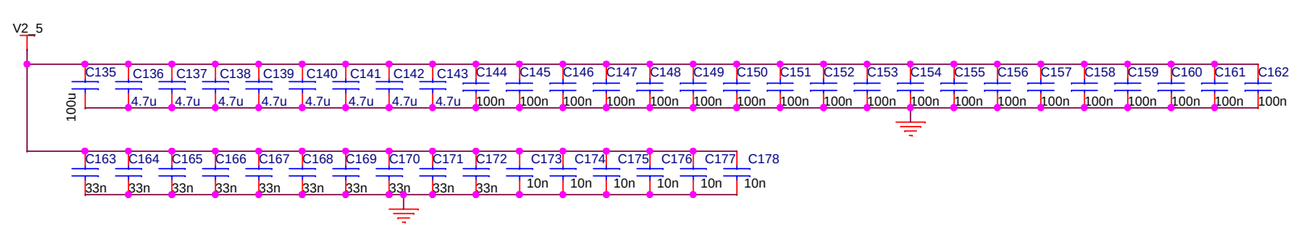
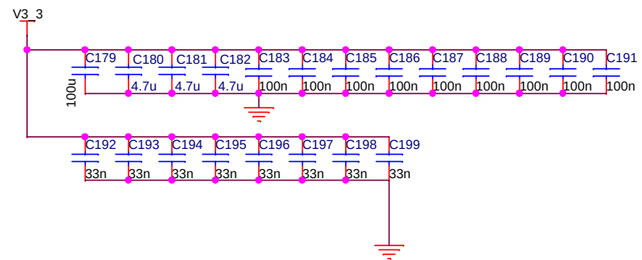
TRB5SC1 - Back-End IO

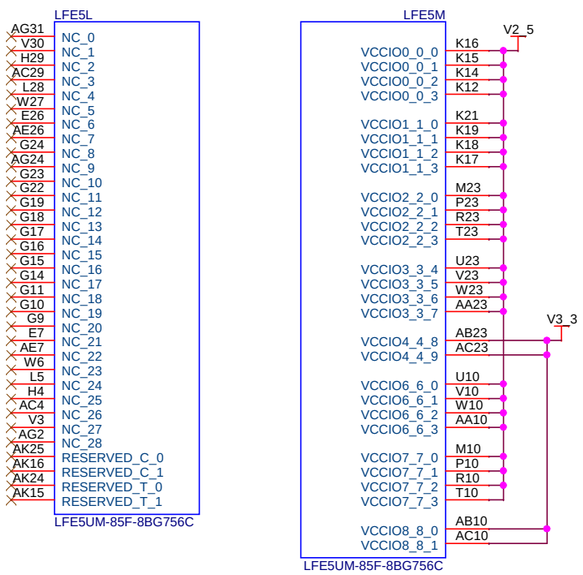
Design: K:\GSIJOB\HADES\TRB5SC\TRB5SC2\TRB5SC2.DSN	
Modified: Monday, March 02, 2020	Size: A3 Page: 5 / 7
Designer: H. Heggen	Layouter: H.Kavan











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TRB5SC1 - POWER BANKS

Design: K:\GSIJOB\HADES\TRB5SC\TRB5SC2\TRB5SC2.DSN
Modified: Monday, March 02, 2020 Size: A3 Page: 6 / 7
Designer: H. Heggen Layouter: H.Kavan

DCDC1V2

V5_5 → R58 4.7k → POK1V2 → D1V2 SML-P11UT red

C208 4.7n, C209 4.7u, C210 100u, C211 100n

ENPIRION_CLOCK → 1k R60 → LLM/SYNC

EN_DCDC → ENABLE

POK1V2 → POK

PVIN, AVIN, AGND, PGND, E-PAD, VOUT, RLLM, SS, VFB

J11, C231 15n

EN6337QI

V1_2_DC

200k R56, 15p C224

C212 100u, C213 4.7u, C214 4.7u, C215 4.7u, C216 4.7u, C217 100n

R63 270k

RB = (0.75 * RA)/(VOUT - 0.75V)

R1: 200kOhm
R2: 270kOhm für 1.305V
R2: 300kOhm für 1.250V

L9 BLM31KN271SH1L

V1_2_LIN

C218 100u, C219 4.7u, C220 4.7u, C221 4.7u, C222 4.7u, C223 100n

ULDO_CORE1

VBIAS

C232 10n, C233 100n, C234 4.7u

IN, IN, BIAS, EN, SS, EP1, EP2, EP3, PG, OUT, OUT, FB, GND, EP4, EP5

TPS74801DRC
SON-10

R57 2.2k, R62 5.6k

V1_1_core

C225 100u, C226 4.7u, C227 4.7u, C228 4.7u, C229 4.7u, C230 100n

results in 1.114V
should be OK for both types of FPGAs

V2_5 → R61 680R → D1V1 SML-P11MT

ULDO_VCCA1

V1_2_LIN

C235 100u, C236 4.7u, C237 4.7u, C238 100n

VBIAS

C244 10n, C245 100n, C246 4.7u

TPS74801DRC
SON-10

results in 1.024V

R64 1.4k, R65 4.99k

V1_1_VCCA

C239 100u, C240 4.7u, C241 4.7u, C242 4.7u, C243 100n

Q1 BSH103 (G, D, S)

Place text on PCB
next to connector:
1: GND
2: 5-5.5V
3: GND

IN_5V5

37203-1AE0-003 PL

V5_5_IN → F4 5A → V5_5

D17 SMBJ5341B-TP

V5_5 → R86 10k → EN_DCDC

DCDC2V6

V5_5 → R69 4.7k → POK2V6 → D2V6 SML-P11UT red

C247 4.7n, C248 4.7u, C249 100u, C250 100n

ENPIRION_CLOCK → 1k R71 → LLM/SYNC

EN_DCDC → ENABLE

POK2V6 → POK

PVIN, AVIN, AGND, PGND, E-PAD, VOUT, RLLM, SS, VFB

J12, C270 15n

EN6337QI

V2_6_DC

R66 160k, C263 15p

C251 100u, C252 4.7u, C253 4.7u, C254 4.7u, C255 4.7u, C256 100n

R73 62k

RB = (0.75 * RA)/(VOUT - 0.75V)

Widerstände für 2.6855V:
R1: 160kOhm
R2: 62kOhm (1%)

L10 BLM31KN271SH1L

V2_6_LIN

C257 100u, C258 4.7u, C259 4.7u, C260 4.7u, C261 4.7u, C262 100n

ULDO2V5

VBIAS

C271 10n, C272 100n, C273 4.7u

IN, IN, BIAS, EN, SS, EP1, EP2, EP3, PG, OUT, OUT, FB, GND, EP4, EP5

TPS74801DRC
SON-10

R68 3.57k, R72 1.69k

V2_5 → R70 680R → D2V5 SML-P11MT

C264 100u, C265 4.7u, C266 4.7u, C267 4.7u, C268 4.7u, C269 100n

DCDC3V4

V5_5 → R75 4.7k → POK3V4 → D3V4 SML-P11UT red

C274 4.7n, C275 4.7u, C276 100u, C277 100n

ENPIRION_CLOCK → 1k R79 → LLM/SYNC

EN_DCDC → ENABLE

POK3V4 → POK

PVIN, AVIN, AGND, PGND, E-PAD, VOUT, RLLM, SS, VFB

J13, C297 15n

EN6337QI

V3_4_DC

R74 160k, C290 15p

C278 100u, C279 4.7u, C280 4.7u, C281 4.7u, C282 4.7u, C283 100n

R81 43k

RB = (0.75 * RA)/(VOUT - 0.75V)

R1: 160kOhm
R2: 43kOhm für 3.54V
R2: 44.2kOhm für 3.46V

L11 BLM31KN271SH1L

V3_4_LIN

C284 100u, C285 4.7u, C286 4.7u, C287 4.7u, C288 4.7u, C289 100n

ULDO3V3

VBIAS

C298 10n, C299 100n, C300 4.7u

IN, IN, BIAS, EN, SS, EP1, EP2, EP3, PG, OUT, OUT, FB, GND, EP4, EP5

TPS74801DRC
SON-10

R76 4.7k, R80 1.5k

V3_3 → R78 1.5k → D3V3 SML-P11MT

C291 100u, C292 4.7u, C293 4.7u, C294 4.7u, C295 4.7u, C296 100n

V2_5 — J2V5 Jumper1x2
V3_3 — J3V3 Jumper1x2
V5_5 — J5V5 Jumper1x2

UPUMP1

V3_4_LIN → C301 100n, C302 4.7u, C308 4.7u

VIN, C1+, C1-, GND, VOUT, C2+, C2-, EN

C306 1u, C307 1u

C303 100n, C304 4.7u, C305 4.7u

VBIAS

5V output, max. 25mA

TPS60241

Place text on PCB next to connector:
3V4
2V6
1V2
GND

IN_LIN1

37204-1AE0-004 PL

F5 5A → V3_4_LIN
F6 5A → V2_6_LIN
F7 5A → V1_2_LIN

D18 SMBJ5341B-TP, D19 SMBJ5341B-TP, D20 SMBJ5341B-TP

6.2V breakdown

Gesellschaft für Schwerionenforschung mbH
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D-64291 Darmstadt
GERMANY
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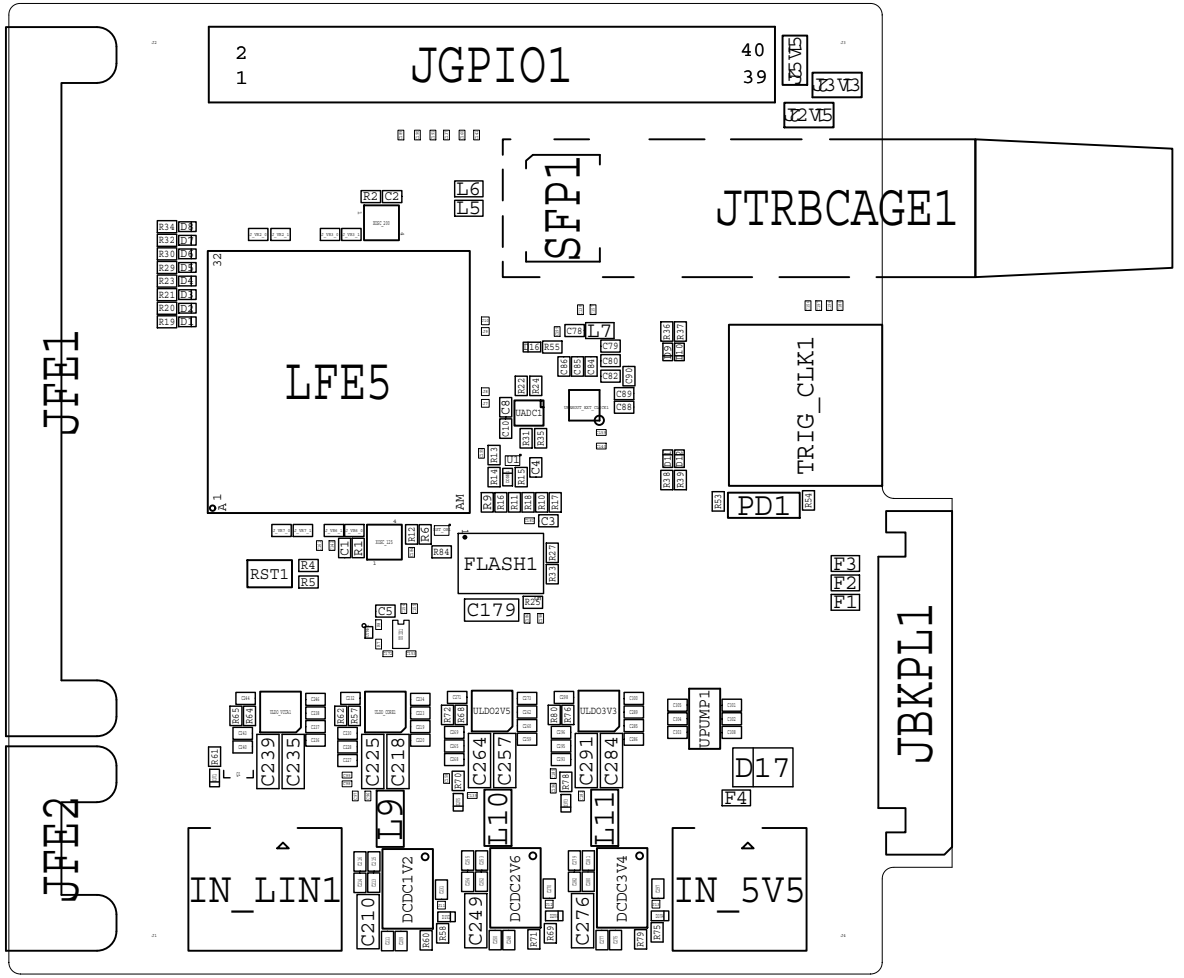
TRB5SC1 - POWER SUPPLY

Design: K:\GSIJOB\HADES\TRB5SC\TRB5SC2\TRB5SC2.DSN	
Modified: Monday, March 02, 2020	Size: A3 Page: 7 / 7
Designer:H. Heggen	Layouter: H.Kavan

Name	Date	Designer	Layouter
TRB5SC2	03.2020	H.Neddermeyer@dpi.de	H.Kayan@dpi.de

Asp

Layer Unterseite



Jobname	Date	Designer	Layouter
TRB5SC2	03.2020	H.Heggen@gsi.de	H.Kayan@gsi.de

Layer Nickname

Ast